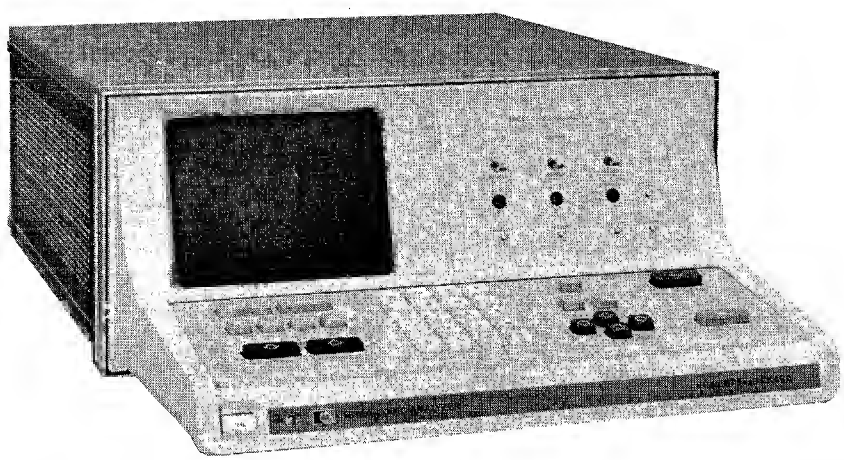
HP 1615A

OPERATING AND SERVICE MANUAL

1615A
LOGIC ANALYZER



HEWLETT PACKARD

HP 1615A

OPERATING AND SERVICE MANUAL

MODEL 1615A
LOGIC ANALYZER

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed **1937A.**

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed **1742A** through **1922A.**

For additional information about serial numbers, see INSTRUMENTS COVERED BY THIS MANUAL in Section I.

Manual Part Number 01615-90904
Microfiche Part Number 01615-90804

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Operating and Service Manual contains information required to install, operate, test, and service the Hewlett-Packard Model 1615A Logic Analyzer.

1-3. SPECIFICATIONS.

1-4. Instrument specifications are listed in table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Table 1-2 lists supplemental characteristics, not specifications but typical characteristics included as additional information for the user.

1-5. INSTRUMENTS COVERED BY THIS MANUAL.

1-6. Attached to the instrument is a serial number tag. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-7. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-8. In addition to change data, the supplement contains information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-9. For information concerning a serial number prefix that is not listed on the title page or in the Manual Change supplement, contact your nearest Hewlett-Packard Office.

1-10. DESCRIPTION.

1-11. The Hewlett-Packard Model 1615A Logic Analyzer offers asynchronous timing diagram measurements and synchronous state measurements for use in the design and troubleshooting of digital systems. Powerful triggering capability, six clock qualifiers, sophisticated delay, occurrence counting, and 256 words of memory assure that the desired timing and state information will be captured.

1-12. Measurement setups are simplified with a menu system which reduces the number and complexity of front panel keys. With the format specification menu, you select the desired mode of operation: timing, state, or simultaneous dual-mode operation. The corresponding trace specification menus then allow you to enter the desired triggering and data parameters.

1-13. MODES OF OPERATION.

1-14. The 1615A offers three basic operating modes: 24-bit state, 8-bit timing, and simultaneous 16-bit state with 8-bit timing. The purpose and use of each of these three modes is described in the following paragraphs.

1-15. 24-BIT STATE MODE.

1-16. In this mode, 256 words of parallel, synchronous data up to 24 bits wide can be accumulated into memory. The bits can be grouped by keyboard selection, and the display of data from each group can be individually read out in either binary, octal, decimal, or hexidecimal formats. Any pattern of the 24 inputs can be established as the trigger point. Part of the trigger pattern can be "don't cares" to establish a range of triggers.

1-17. 8-BIT TIMING MODE.

1-18. In this mode, asynchronous data is clocked into memory. The clock rate for data acquisition can be selected in a 1, 2.5, 5 sequence from 50 ns to 500 ms per clock period. On the timing diagram, the clock period is displayed on screen along with the related horizontal time scale. The time between any two samples in memory is displayed in a direct readout on the CRT.

1-19. The eight lines on pod 1 are the only active lines in the eight-bit timing mode. The displayed channels can be ordered in any arrangement by keyboard selection. The memory in this mode is eight bits wide, 256 words deep. Glitches are displayed as bright vertical bars along each separate channel.

1-20. The trigger point is shown by a set of short, vertical lines from top to bottom on the display. Up to three ORed patterns of the 8 bits (along with don't cares) can be established as the trigger requirement, or the Boolean NOT of a particular pattern can be selected (this allows triggering on a fault in a status word). Since the trigger pattern is truly asynchronous, transient states can provide false triggers. To avoid triggering on a false pattern, the duration of the trigger pattern is selectable between 15 ns and 2000 ns. Glitch occurrences on any input line may be added to the trigger requirements. An external trigger line can also be connected through the clock pod. Either time delay or external clock delay can be added to the trigger specification, if desired.

1-21. 16-BIT AND 8-BIT MODE.

1-22. In this mode, eight bits of asynchronous timing data is captured at the same time that 16 bits of synchronous state data is captured. The logic analyzer can capture timing sequences that occur before or after a particular state, or state sequences occurring before or after a timing event. This measurement allows correlation of activity on control lines, address decoder outputs, and asynchronous I/O structures with specific states in program flow.

1-23. Four instrument triggering arrangements are available in the 16-bit and 8-bit mode of operation: 16 bit arms or triggers 8 bit, and 8 bit arms or triggers 16 bit. If 8 bit triggers 16 bit is selected, the 1615A captures data as soon as the asynchronous event is recognized. This enables observation of state information related to a timing event such as an interrupt or glitch. By selecting 8 bit arms 16 bit, the 1615A will capture data at a specific point in program flow, but only after a particular asynchronous event has occurred, such as a service request.

1-24. The 16 bit arms or triggers 8 bit specification allows the capture and display of timing information related to a particular point in program flow. This can be used to look at the conditions of lines on an input port for a short time prior to reading the port to ensure that data is valid. By using the end-display mode, the timing information can be captured prior to the reading of the port.

1-25. ACCESSORIES SUPPLIED.

1-26. The following accessories are supplied with the 1615A:

Four 8-bit probes (HP Model 10248B) with leads and tips (three for data, one for clock, qualifiers, and external trigger)

One 2.3 m (7.5 ft) power cord (refer to Section II)

One extender board (HP Part No. 01615-66512) installed inside 1615A instrument.

One Operating and Service Manual

1-27. RECOMMENDED TEST EQUIPMENT.

1-28. Equipment required to maintain the Model 1615A is listed in table 1-3. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-1. Specifications

CLOCK, QUALIFIER, AND DATA INPUTS

REPETITION RATE: to 20 MHz.

INPUT RC: 50 kΩ shunted by ≤14 pF at the probe tip.

INPUT THRESHOLD: TTL, fixed at approx 1.5 V; variable ±10 Vdc.

MAXIMUM INPUT: 15 V to 15 V.

MINIMUM INPUT

Swing: 0.6 V.

Clock Pulse Width: 20 ns at threshold level.

Setup time: time data must be present prior to clock transition 20 ns.

Hold Time: time data must be present after clock transition, zero.

ASYNCHRONOUS OPERATION

SAMPLE RATE: 2 Hz to 20 MHz.

DATA SKEW: 9 ns maximum.

MINIMUM DETECTABLE GLITCH: 5 ns width and exceeding threshold by 30% of ac swing or 250 mV, whichever is greater.

GLITCH TRIGGER: on any selected channel(s), if a glitch is captured, the glitch is AND'd with the asynchronous pattern trigger.

EXTERNAL TRIGGER PULSE WIDTH: 5 ns minimum with 30% peak overdrive or 250 mV whichever is greater.

PATTERN TRIGGER: any 8-bit pattern. Trigger duration required is selectable 15, 50, 100, 200, 500, 1000, or 2000 ns ±15 ns or 15% whichever is greater.

TRIGGER OUTPUTS (Rear Panel)

16/24 BIT TRIGGER OUTPUT

Level: high, ≥2 V into 50Ω; low, ≤0.4 V into 50Ω.

Pulse Duration: approx 25 ns.

Delay from Input Clock: approx 85 ns.

16/24 BIT TRACE POINT OUTPUT

Level: high, ≥2 V into 50Ω; low, ≤0.4 V into 50Ω.

Pulse Duration: starts at beginning of trace and ends at the trigger point (pattern trigger plus delay).

Delay from Input Clock: approx 85 ns.

8 BIT PATTERN OUTPUT

Level: high, ≥2 V into 50Ω; low, ≤0.4 V into 50Ω.

Pulse Duration: pattern duration minus asynchronous trigger duration width.

Delay from Pattern at Probe: approx 75 ns plus asynchronous trigger duration width.

GENERAL

MEMORY DEPTH: 256 data transactions (in timing display mode, 249 samples are displayed).

Table 1-2. Supplemental Characteristics

SELECTABLE DELAYS

SYNCHRONOUS TRIGGER DELAY: to 999 999 clocks.
SYNCHRONOUS TRIGGER OCCURRENCES: to 999 999.
ASYNCHRONOUS TIME DELAY: to 1 048 575 times sample period.

POWER

100, 120, 220, 240 Vac; —10% to +5%; 48 to 66 Hz; 230 VA max.

DIMENSIONS

see outline drawing.

OPERATING ENVIRONMENT

TEMPERATURE: 0°C to 55°C.
HUMIDITY: up to 95% relative humidity at +40°C.
ALTITUDE: to 4600 m (15 000 ft).
VIBRATION: vibrated in three planes for 15 min. each with 0.3 mm (0.015 in) excursions, 10 to 55 Hz.

WEIGHT

NET: 19.1 kg (42 lb).
SHIPPING: 23.6 kg (52 lb).

ACCESSORIES SUPPLIED

four 8-bit Model 10248B probes with probe leads and tips (three for data and one for clock, qualifiers, and external trigger) one 2.3 m (7.5 ft) power cord, one operating and service manual.

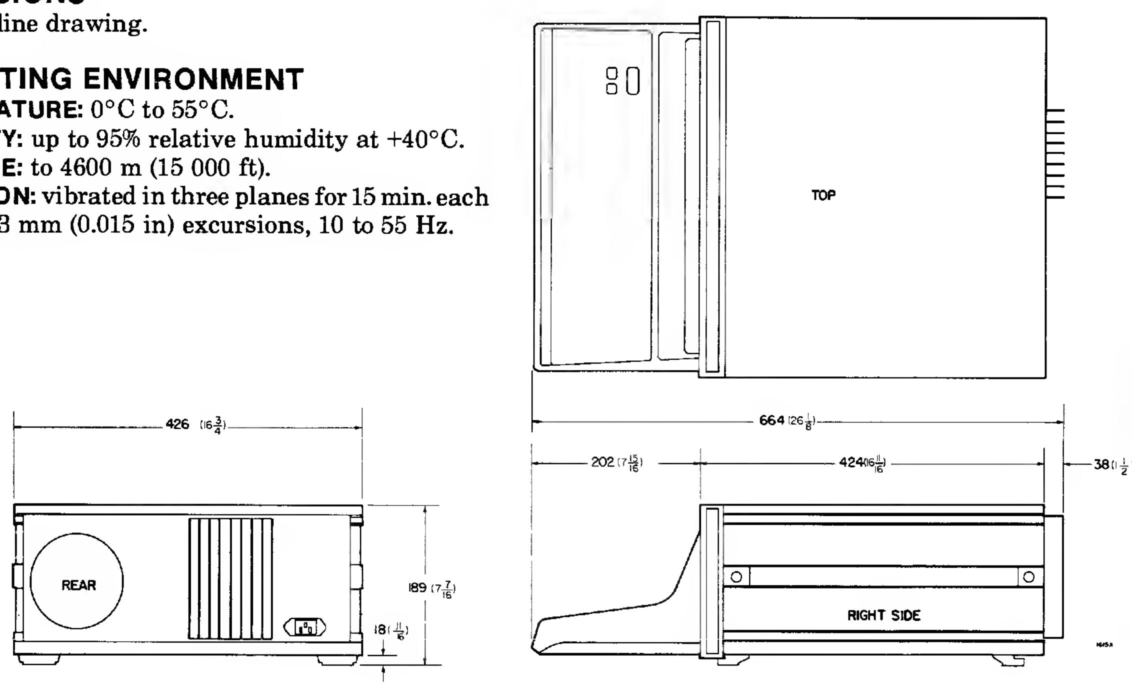


Table 1-3. Recommended Test Equipment

Instrument	Critical Specification	Recommended Model	Use*
Pulse Generators (2)	External trigger dc to 50 MHz, variable >10 ns pulse width	HP 8013B	P
5-ns Pulse Generator	5-ns pulse width, 30-ns pulse period, TTL levels	HP 8007B	P
Multimeter	±1000 Vdc range, 0.1% accuracy	HP 3465A	P,T
Oscilloscope	275 MHz BW, dual channel	HP 1725A	P,A,T
Logic State Analyzer	Pattern recognition and state display	HP 1611A Option 080	T
Logic Pulser	Pulse logic circuits	HP 10526T	T

Table 1-3. Recommended Test Equipment (Cont'd)

Instrument	Critical Specification	Recommended Model	Use*
Logic Probe	Monitor digital IC's	HP 10525T	T
BNC-to-alligator Clip Adapters (3)		HP Part No. 8120-1292	P
BNC Tee Connectors (2)		HP Part No. 1250-0781	P
Current Tracer		HP 547A	T
Logic Signature Analyzer	No Substitute	HP 5004A or ET 9254	T
LCR Meter	Capacitance, 0 to 25 pF	HP 4332A	P

*P = Performance Test, A = Adjustment, T = Troubleshooting

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information and instructions for installing the Model 1615A. Included are initial inspection procedures, power and grounding requirements, and instructions for repacking for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

2-6. POWER REQUIREMENTS.

2-7. The 1615A requires a power source of 100, 120, 220, or 240 Vac; —10%, +5%; single-phase; 48 to 66 Hz; 230 VA maximum.

CAUTION

The instrument may be damaged if the LINE switch pair on the rear panel is not set to match the input voltage in use.

2-8. LINE VOLTAGE SELECTION.

2-9. The LINE switch pair on the rear panel selects either 100-, 120-, 220-, or 240-volt operation. To check or change the position of the LINE switch pair, proceed as follows:

a. Remove input power cord (if connected).

b. For 100-volt or 120-volt operation, set the LINE switch pair to 100 V or 120 V respectively. Then install the 4-ampere fuse for F1 (located beside the line power connector).

c. For 220-volt or 240-volt operation, set the LINE switch pair to 220 V or 240 V as applicable and install a 2-ampere fuse for F1 (located beside the line power connector).

d. Reconnect power cord.

2-10. POWER CORDS AND RECEPTACLES.

2-11. Figure 2-1 illustrates the standard configurations used for HP power cords. The HP part number directly above each drawing is the part number for an instrument power cord equipped with a connector of that configuration. If the appropriate power cord is not included with the instrument, notify the nearest HP Sales/Service Office and a replacement cord will be provided.

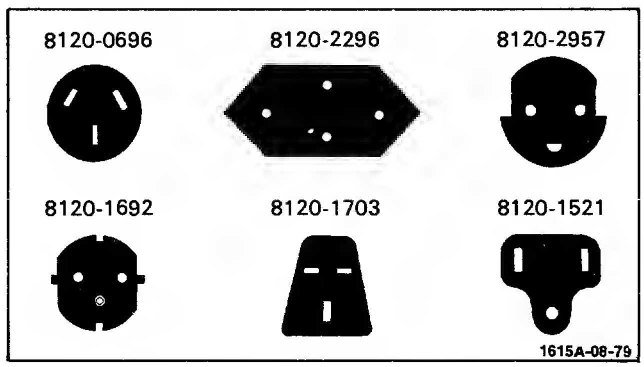
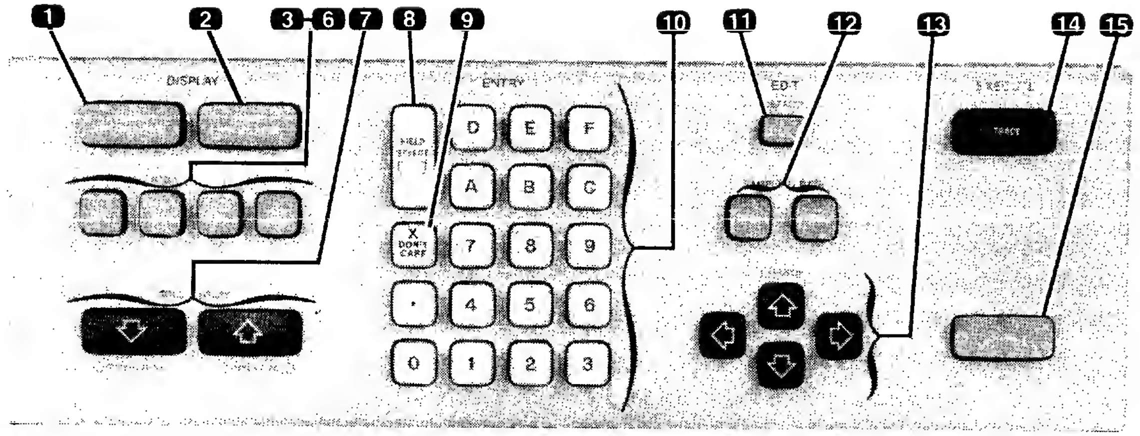


Figure 2-1. Power Cord Configurations

2-12. REPACKING FOR SHIPMENT.

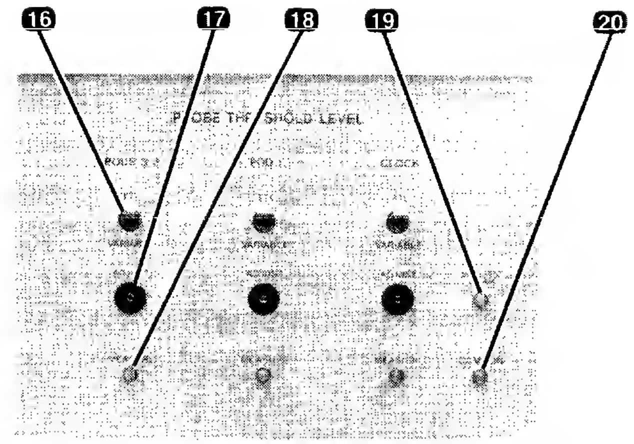
2-13. If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-14. Use the original shipping carton and packing material. If the original packing material is not available, the Hewlett-Packard Sales/Service Office will provide information and recommendations on materials to be used.

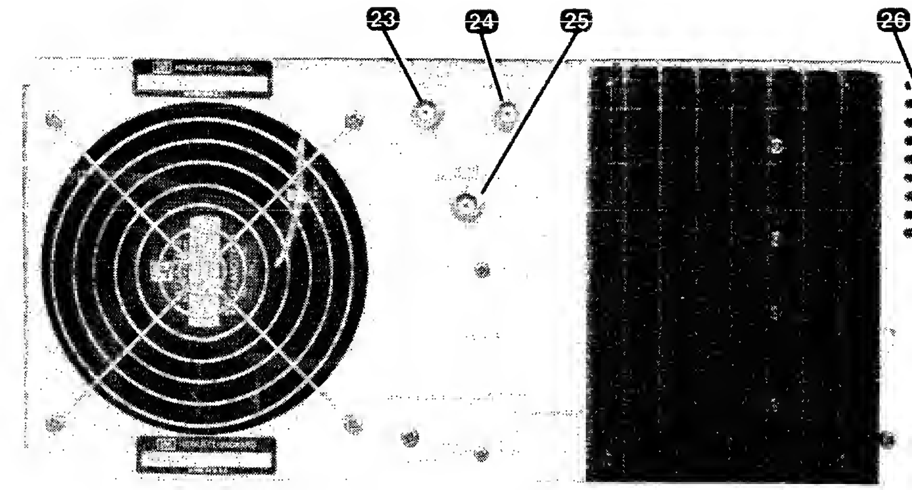


KEYBOARD FEATURES

1615A
FRONT RAIL



PROBE THRESHOLD LEVEL GROUP



REAR PANEL FEATURES

DISPLAY GROUP

1 FORMAT SPECIFICATION. Calls up a menu which allows you to select the operating mode, clock slope, logic polarity, and number base parameters. It also permits arranging up to 24 input channels into labelled groups.

2 TRACE SPECIFICATION. Calls up a display menu in which you can specify trigger requirements, position of the trigger relative to captured data within the memory, and the clock parameters.

3 LIST. Calls up a display window of 15 lines of the data captured in the 256-line memory.

4 TIMING DIAG. Calls up a timing diagram of up to eight lines of the 256-bit memories. This mode permits precise time measurements between points on the traces. The trigger point is displayed as a set of short vertical bars. Glitch occurrences are captured in a separate memory and displayed as bright vertical bars on the individual traces. In this mode, X10 magnification can be selected for any segment of a displayed trace to permit improved display resolution. Probe pod 1 supplies the signals for timing diagram display.

5 CHAN SEQ. This key offers the convenience of returning a timing diagram to its most simple form (lines 0 through 7 from top to bottom) after a special sequence of lines has been arranged on the display.

6 AT TRIG WORD. In the list mode, pressing this key brings the display to the area of the trigger word. If the trigger word starts the display, it will be the first line of the display. If END was selected, the trigger word will be the last line displayed. In a timing diagram the brightened segment will switch immediately to the trigger word when AT TRIG WORD is pressed. If X10 magnification is being used, the display window will move to the segment which includes the trigger word. If so much trigger delay was selected that the trigger word is not in memory, pressing AT TRIG WORD will bring an error message on screen (WARNING — TRIGGER NOT IN MEMORY).

7 ROLL DISPLAY. In the list mode, this set of keys moves the display window up or down through the 256-bit memory. In the timing diagram mode, this set of keys moves the brightened trace segment left or right across the display (for relative time measurements or selection of an area to be expanded). It also moves the display window in X10 magnification.

ENTRY GROUP

8 FIELD SELECT. Permits selection of variables in the field contents. This key is used to make selections of variables within inverse fields which contain brackets ([ ]). It is also used to set the zero reference point for making point-to-point time measurements.

9 X DON'T CARE. In entry fields, X accepts all allowed digit values (0 through 7 in octal, 0 through F in hex, etc.). In label assignment fields, X disables the channel. An unused channel is not included in any other label reference.

10 A-F, ., 0-9. Alphanumeric keys for entering information into all entry fields on the display.

EDIT GROUP

11 DEFAULT. Returns the currently displayed menu to its simplest form.

12 SAMPLE PERIOD. Selects the repetition rate of the internal clock. The clock rate may be incremented or decremented from 50 ns to 500 ms per clock (in a 1, 2.5, 5 sequence) in any display where the internal clock rate is shown.

13 CURSOR. Set of switches used to move the blinking cursor to the desired location within the menu.

EXECUTE GROUP.

14 TRACE. Initiates a search in logic flow to find and capture data that corresponds to the parameters defined in the specification menus, then displays captured data. Pressing TRACE one time initiates a single trace. Holding the key down places the 1615A in a continuous trace mode, permitting observation of dynamic program flow.

15 STOP. Stops any trigger search or data acquisition which is in process. In order to stop a continuous trace mode, the STOP must be pressed once to go to the in-process mode, and then a second time to abort the trace.

PROBE THRESHOLD LEVEL GROUP.

16 TTL/VARIABLE. When this switch is set to TTL, its associated probe pod(s) is biased to operate at TTL (1.4 V) threshold levels. In the VARIABLE position, the probe pod bias is adjusted to the required voltage at the MEASURE test point.

17 ADJUST. Adjustment for setting logic threshold level to the desired amplitude, offering a range from —10 V to +10 V.

18 MEASURE. A test point for measuring probe threshold level voltage during adjustment.

19 SELF-TEST CLOCK. A test point for obtaining a clock signal during self-test procedures and troubleshooting.

20 COMMON. A grounding point for use when making threshold voltage adjustments and using the SELF-TEST CLOCK.

21 LINE. Applies line power to the instrument.

22 ON. Lights when operating power is applied to the 1615A.

REAR PANEL GR

23 16/24 BIT TRIG output provides a trigger pattern p Trigger pulse ge the condition of within the 1615A synchronize an os lar point in data

24 16/24 BIT TRACE beginning of a t TRACE key is p searching for a tr recognition of the the delay period can be used to pro end-trigger meas

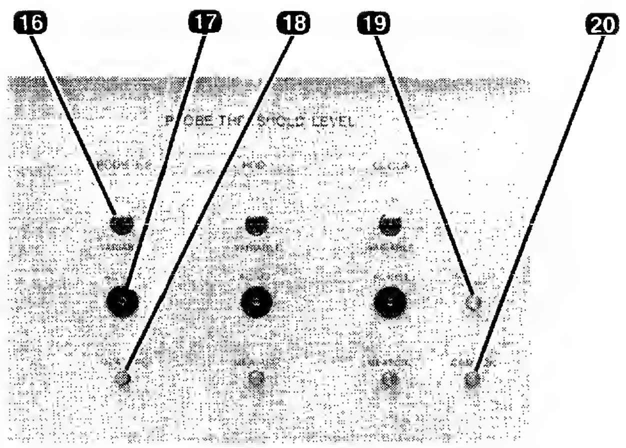
25 8 BIT PATTERN the selected trigge ing measurement

26 LINE SWITCH P arrangement for

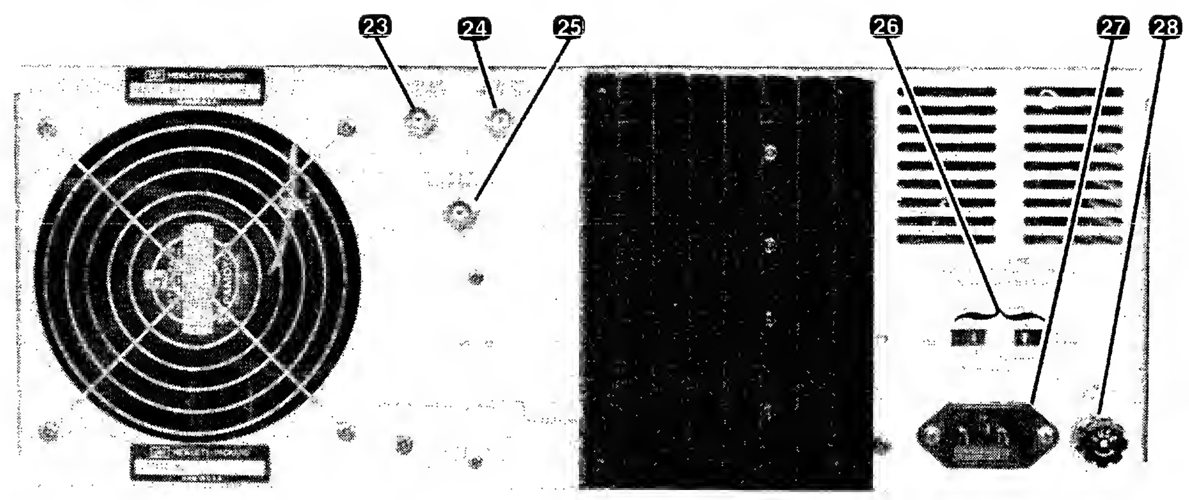
27 LINE CONNECT power.

28 LINE FUSE. Cont

Figure 3-1.
Operating Controls, Indicators, and Connectors



PROBE THRESHOLD LEVEL GROUP



REAR PANEL FEATURES

(9) **X DON'T CARE.** In entry fields, X accepts all allowed digit values (0 through 7 in octal, 0 through F in hex, etc.). In label assignment fields, X disables the channel. An unused channel is not included in any other label reference.

(10) **A-F, ., 0-9.** Alphanumeric keys for entering information into all entry fields on the display.

EDIT GROUP

(11) **DEFAULT.** Returns the currently displayed menu to its simplest form.

(12) **SAMPLE PERIOD.** Selects the repetition rate of the internal clock. The clock rate may be incremented or decremented from 50 ns to 500 ms per clock (in a 1, 2.5, 5 sequence) in any display where the internal clock rate is shown.

(13) **CURSOR.** Set of switches used to move the blinking cursor to the desired location within the menu.

EXECUTE GROUP.

(14) **TRACE.** Initiates a search in logic flow to find and capture data that corresponds to the parameters defined in the specification menus, then displays captured data. Pressing TRACE one time initiates a single trace. Holding the key down places the 1615A in a continuous trace mode, permitting observation of dynamic program flow.

(15) **STOP.** Stops any trigger search or data acquisition which is in process. In order to stop a continuous trace mode, the STOP must be pressed once to go to the in-process mode, and then a second time to abort the trace.

PROBE THRESHOLD LEVEL GROUP.

(16) **TTL/VARIABLE.** When this switch is set to TTL, its associated probe pod(s) is biased to operate at TTL (1.4 V) threshold levels. In the VARIABLE position, the probe pod bias is adjusted to the required voltage at the MEASURE test point.

(17) **ADJUST.** Adjustment for setting logic threshold level to the desired amplitude, offering a range from —10 V to +10 V.

(18) **MEASURE.** A test point for measuring probe threshold level voltage during adjustment.

(19) **SELF-TEST CLOCK.** A test point for obtaining a clock signal during self-test procedures and troubleshooting.

(20) **COMMON.** A grounding point for use when making threshold voltage adjustments and using the SELF-TEST CLOCK.

(21) **LINE.** Applies line power to the instrument.

(22) **ON.** Lights when operating power is applied to the 1615A.

REAR PANEL GROUP.

(23) **16/24 BIT TRIG OUT.** During state analysis, this output provides a trigger pulse whenever the state trigger pattern plus selected delay is recognized. Trigger pulse generation continues regardless of the condition of the data acquisition circuitry within the 1615A. This trigger pulse can be used to synchronize an oscilloscope for observing a particular point in data flow.

(24) **16/24 BIT TRACE OUT.** Provides a high state at the beginning of a trace of synchronous data (when TRACE key is pressed and the machine begins searching for a trigger). This output resets low after recognition of the synchronous trigger pattern plus the delay period or occurrence count. This output can be used to provide a clock-stopper signal during end-trigger measurements.

(25) **8 BIT PATTERN OUT.** Provides a trigger pulse when the selected trigger pattern is recognized during timing measurements.

(26) **LINE SWITCH PAIR.** Selects proper input circuit arrangement for input voltage in use.

(27) **LINE CONNECTOR.** Connection for operating power.

(28) **LINE FUSE.** Contains input operating power fuse.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section provides operating information, explains functions of 1615A controls, connectors, and indicators and describes measurement capabilities of the instrument.

3-3. PANEL FEATURES.

3-4. The 1615A keyboard and panel features are described in figure 3-1. Description numbers match the numbers on the illustration.

3-5. OPERATING INFORMATION.

3-6. The 1615A offers two logic analyzers in one: a synchronous state analyzer and an asynchronous timing analyzer. Each analyzer captures data independently from the other analyzer, although triggering of the two analyzers is related.

3-7. **STATE ANALYZER.** The 1615A can be used for state analysis. It will capture and display up to 256 bytes of an operating program. It can capture bytes up to 24 bits wide (up to 16 bits wide when the timing analyzer is also in use).

3-8. In state analysis, the incoming data is synchronized with the incoming clock. Trigger delays are measured in numbers of incoming clocks. The state analyzer does not have the capability to detect glitches.

3-9. **TIMING ANALYZER.** The 1615A can generate a timing diagram of the data obtained on up to eight input lines (one 256-bit trace for each input line). The 1615A generates several internal clocks at different rates for capture of a trace. Additionally, an external clock can be used, if desired. Trigger delays are measured directly in units of time when operating with one of the internal clocks. Delays are measured as a number of clocks when operating with an external clock. The timing analyzer is capable of capturing glitches and displaying them as intensified bars on timing diagrams.

3-10. SYNCHRONOUS VS ASYNCHRONOUS OPERATION.

3-11. **SYNCHRONOUS ANALYSIS (See figure 3-2).** When the 1615A is configured as a synchronous analyzer, it gathers data bytes which are synchronized with a clock. The clock is supplied from an external source. It need not be periodic as long as it is synchronized with the data (D0 and D1) to be analyzed. Trigger recognition occurs when the clock arrives at the same time that the states on the data lines match the trigger pattern specified.

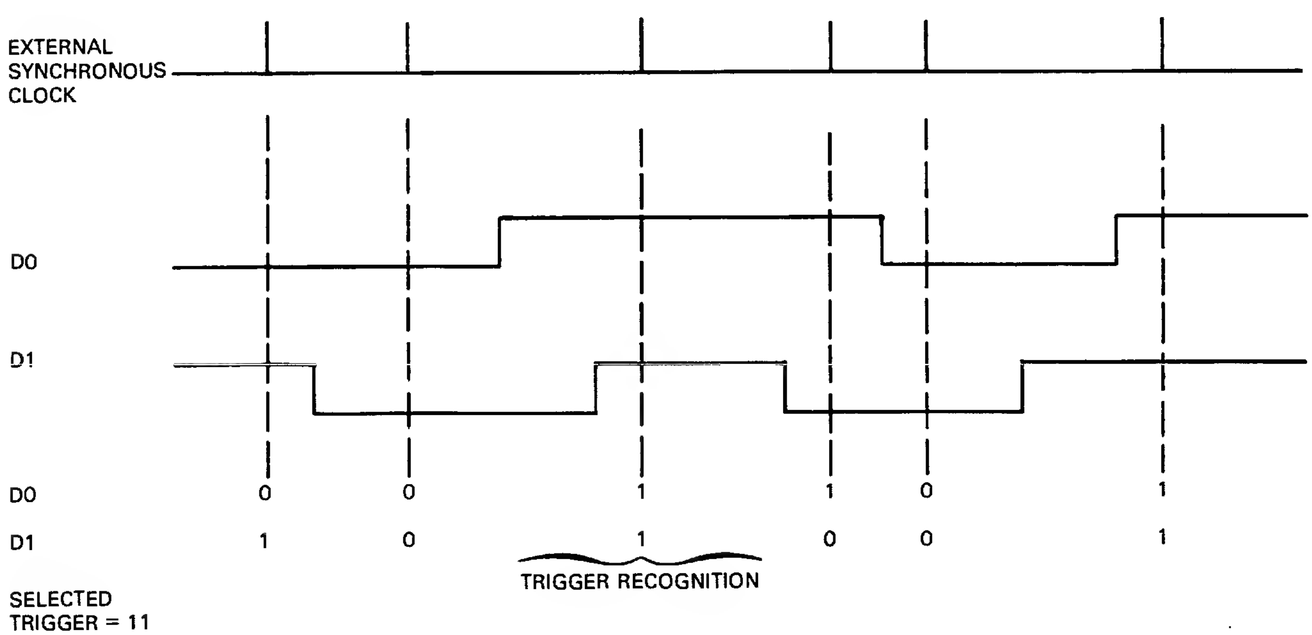


Figure 3-2. Synchronous Operation

3-12. ASYNCHRONOUS ANALYSIS (See figure 3-3). When the 1615A is configured as an asynchronous analyzer, the clock is not synchronized with the incoming data. The clock is periodic and is used for time measurement. The states on the data lines are captured when each clock occurs until 256 sequential states have been obtained in memory. After the run, a trace is made for each data line showing all 256 states on the CRT as a plot of line state with respect to time.

3-13. In the timing analyzer, trigger recognition is not a clock function. Anytime that the logical set specified as the trigger word appears on the data lines, the 1615A begins a measurement of time duration. The time duration is selected by the operator prior to the run. If the logical set changes before the end of the specified duration, the 1615A will reset immediately and begin a new search for the trigger word. When the logical set remains stable for the selected duration, the 1615A recognizes its trigger.

3-14. In START trace modes, data acquisition is inhibited until after trigger recognition occurs. In modes where trigger recognition ends the trace, data acquisition begins immediately as soon as the run begins, and data acquisition stops when the trigger is recognized.

3-15. THE MENU CONCEPT.

3-16. Usually, instruments capable of complex measurements have equally complex front panels. By contrast, the 1615A is capable of complex measurements but has a simple keyboard. Control complexity is replaced with a set of menus. Each menu displays a set of measurement parameters to be selected by the operator. By positioning a movable cursor (an alternating display of video and inverse video), the operator selects one of the parameters in the menu. Then he enters the desired conditions, and moves the cursor on to the next parameter. If the cursor is positioned in a field enclosed by brackets (such as MODE, CLOCK SLOPE, LOGIC POLARITY, or BASE), selections are made by pressing the FIELD SELECT key. If the cursor is positioned in a field without brackets, entries are made with the other keys in the ENTRY block on the keyboard.

3-17. OPERATING PROCEDURES.

3-18. INSTRUMENT CONNECTIONS (See figure 3-4).

3-19. Connect operating power to the rear-panel connection on the 1615A. Make sure that power-selector switches above the power connector are properly set for the voltage in use.

3-20. Connect the probe cables to pod connectors under the keyboard by sliding each connector keeper to the left, pressing the connector into the receptacle, and then sliding the keeper to the right. Make certain that the proper probe cable is connected to each input receptacle.

3-21. Connect pod 1 to the signals to be analyzed either by timing diagrams or by digital list. Either synchronous state or asynchronous timing tests may be made by the 1615A through the eight probes in pod 1.

3-22. Connect pods 2 and 3 to the signals to be analyzed by digital lists. The 1615A makes synchronous state tests through the eight probes in each of these two pods.

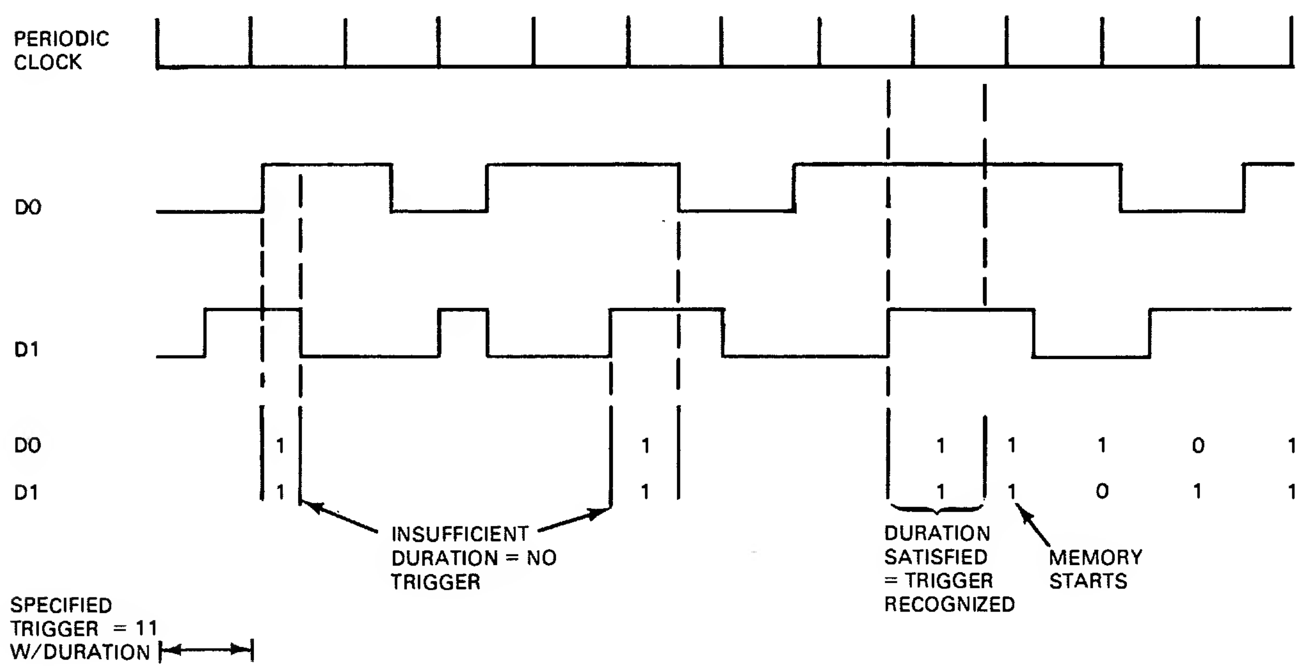


Figure 3-3. Asynchronous Operation

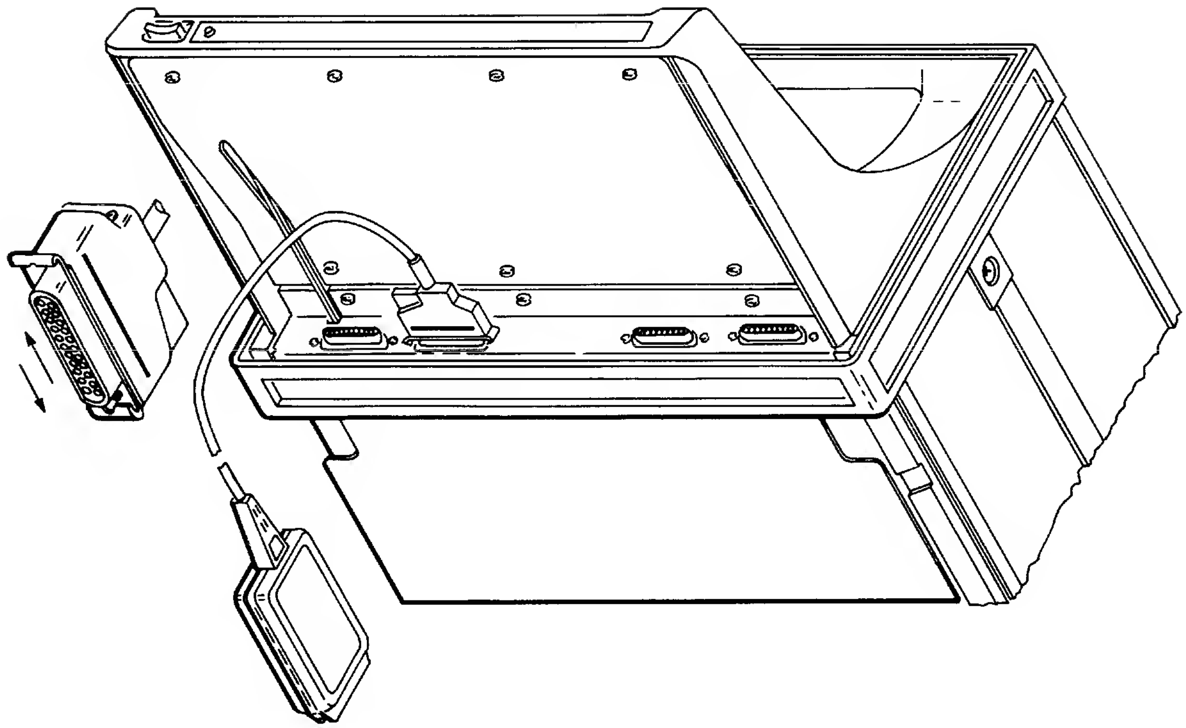


Figure 3-4. Probe Cable Installation

3-23. Connect clock probe to the enternal clock signal source, if used. An external clock signal is required for all synchronous measurements. The 1615A has an internal clock which may be used for obtaining timing diagrams. Connect the clock probe as follows:

a. Connect the CLOCK terminal to the external clock signal.

b. Connect qualifier lines (QUAL 0 through 5) to the sources of qualifier signals, if used.

c. Connect EXT TRIG terminal to the source of an external trigger if desired for obtaining timing diagrams.

d. Connect the inner ground terminal to a source of signal ground.

e. Connect the outer ground terminal to a source of signal ground, except when clock signals are obtained through the external probe wires. When external wires are used, the outer ground terminal must be left open; this prevents glitch generation in the external wires.

f. Ground all unused probe cables on all pods. Unused probe inputs may pick up glitches if left ungrounded.

g. Connect cables to any of the three rear-panel BNC terminals if triggering of external instruments is desired. Refer to the rear-panel group described in figure 3-1 for the signal characteristics of each rear panel BNC.

3-24. INSTRUMENT TURN ON.

3-25. Power is applied to the 1615A by pressing the LINE switch. The ON lamp lights, and the 1615A executes the power-up self test. When self test is complete, the format specification for the 24-bit mode appears on screen. A successful self test is assured by the statement POWER UP COMPLETE in the upper, right-hand corner of the display.

NOTE

If the self test fails, the 1615A will display TEST FAILED, STATUS = (3-digit failure code). Refer to Section VIII of this manual for an explanation of the failure codes.

3-26. The probe threshold level panel provides separate adjustments for pod 1, pods 2 and 3 combined, and for the clock pod. Adjust the probe threshold voltage as follows:

a. If the probe pods are connected to TTL circuitry, set the TTL/VARIABLE switches to TTL. This establishes the proper probe threshold voltage (+1.4 V) for measuring signals with TTL levels.

b. If the probe pods are connected to logic circuitry operating on other than TTL levels, set the TTL/VARIABLE switches to VARIABLE. Connect a voltmeter to the associated MEASURE test point. Then adjust the associated ADJUST control for an indication of the proper threshold voltage for the logic circuitry under analysis. The ADJUST control can select any voltage between —10 V and +10 V.

3-27. 24-BIT SYNCHRONOUS STATE MEASUREMENTS.

3-28. In the 24-bit mode, up to 24 lines of synchronous activity can be monitored. This mode of operation uses the following two menus: 24-bit Format Specification (figure 3-7), and 24-bit Trace Specification (figure 3-8). In the 24-bit Format Specification menu, the operator can choose the format for combining and displaying information. In the 24-bit Trace Specification menu, the operator selects the type of data and area of program execution to be captured. Each menu can be obtained on the 1615A display by pressing the appropriate key in the DISPLAY group on the keyboard.

3-29. SYNCHRONOUS STATE CAPTURE AND DISPLAY. Press the TRACE key. The 1615A will capture 256 bytes of synchronous data and display a trace list. Figure 3-9 shows a typical trace list.

3-30. SEPARATING ADDRESS AND DATA. The synchronous state analyzer can be set up to capture and display address and data bus information in separate, related listings. By selecting the 24-bit Format Specification and labeling the probes connected to address bus A and the probes connected to the data bus C, the 1615A will provide a display which includes separate lists for each bus while still relating them on the display according to each clock. By separating the address bus and data bus in different lists, the logic polarity for each bus and the number base used for presentation can be assigned to each of the two buses.

3-31. DELAY APPLICATIONS. The state DELAY mode is used to delay data capture a known number of clocks from the trigger. One application is displaying a series of consecutive 256-byte pages of a very long program. This may be accomplished by making several traces of program activity, each trace with an additional 256 bytes of delay.

3-32. The trigger OCCUR delay could be used to obtain any particular pass through a program loop. By selecting an address within the loop as the trigger word and then specifying delay by trigger OCCURrences, any desired pass through the loop could be captured and displayed, up to 999 999 occurrences.

3-33. CLOCK QUALIFIER APPLICATIONS. Sometimes it is necessary to capture only that activity in a specific area, such as activity involving a particular ROM in a system. The clock qualifier simplifies this information capture. By connecting one of the clock qualifier lines to the chip-select pin on the ROM, and then setting the clock qualifier on the trace specification to only recognize clocks which occur when the chip-select is in the active state, a listing of activity isolated to those program steps involving the ROM can be obtained.

3-34. Two qualifier words may be used to specify two OR'd conditions for acceptable data, such as capturing only I/O reads or I/O writes when data acquisition is to be limited to I/O activity. Qualifier line 1 could be connected to the read line, and qualifier line 2 connected to the write line. Additionally, qualifier line 3 could be connected to a line which is active only when an I/O operation is in process, such as $\overline{M}$/I/O. By selecting the following two qualifier words: XXX1X1 and XXX11X, only reads (line 1) or writes (line 2) will be clocked into the 1615A state memory when an I/O operation (line 3) is being implemented.

3-35. ACTIVITY PRECEEDING A KNOWN EVENT. Sometimes it is necessary to observe activity leading up to a known event. Figure 3-5 shows a program sequence which contains three possible paths. The 1615A can be used to determine exactly which path was selected during program execution. By setting the 1615A to trigger on the first event following the convergence of the three paths, and selecting the END trace mode, the 1615A will capture and display the activity that led up to the trigger event. By including some delay with the END trigger specification, the trigger event can be positioned within the 1615A memory so that activity before and after the trigger event can be observed on the same display.

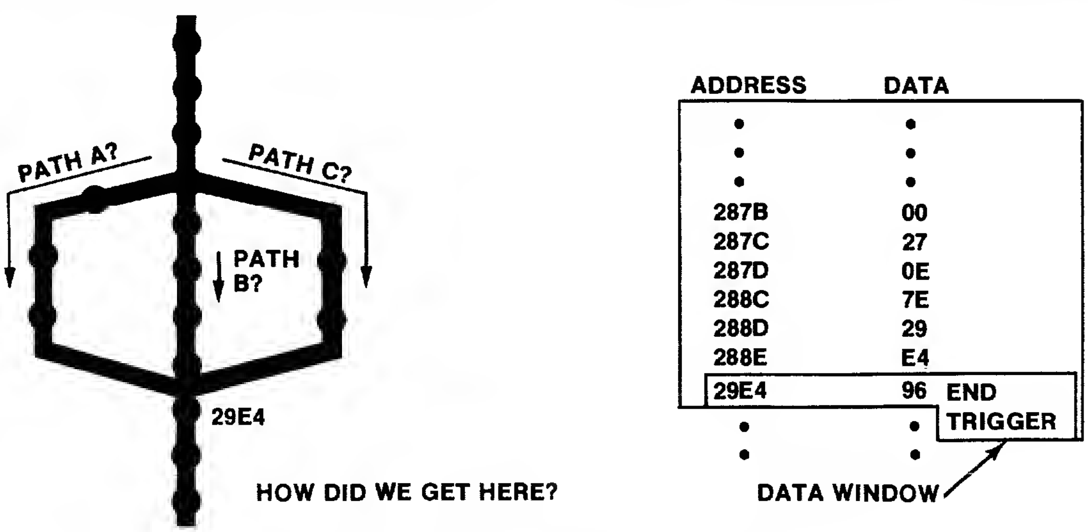


Figure 3-5. Activity Preceeding a Known Event

3-36. APPLICATION FOR TRACE TRIGGER EVENTS. When a specific quantity changes with each pass through a loop, this change can be observed by using TRACE TRIGGER EVENTS plus delay. The trigger word should be a non-changing address in the loop. The delay is used to offset data capture to the changing event to be observed. As the program runs, one event is captured each time that the loop occurs. The 1615A displays the sequential changes in the event being monitored.

3-37. DISPLAYING A PARTICULAR PASS THROUGH A LOOP. Sometimes it is desireable to observe program activity during a particular pass through a program loop (figure 3-6). The 1615A enables the operator to capture and display any desired pass through such a loop. The 1615A can be set to recognize a particular address within the loop as the trigger word. Then by specifying delay as a number of trigger recognitions, the desired pass can be captured and displayed.

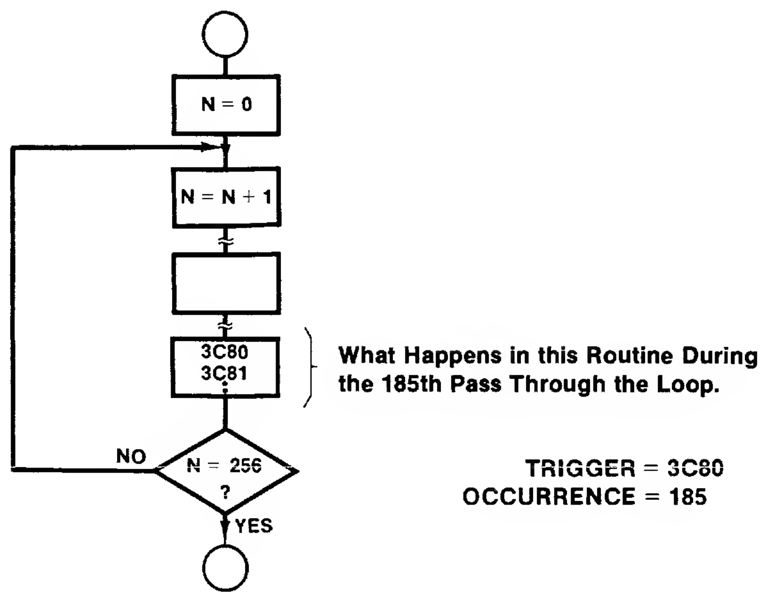
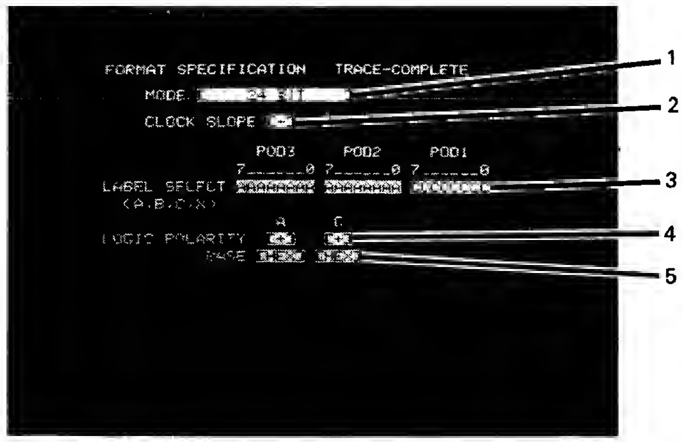


Figure 3-6. Viewing a Particular Pass Through a Loop



1. **MODE select:** Move cursor to this field and press FIELD SELECT key to obtain 24 BIT mode.

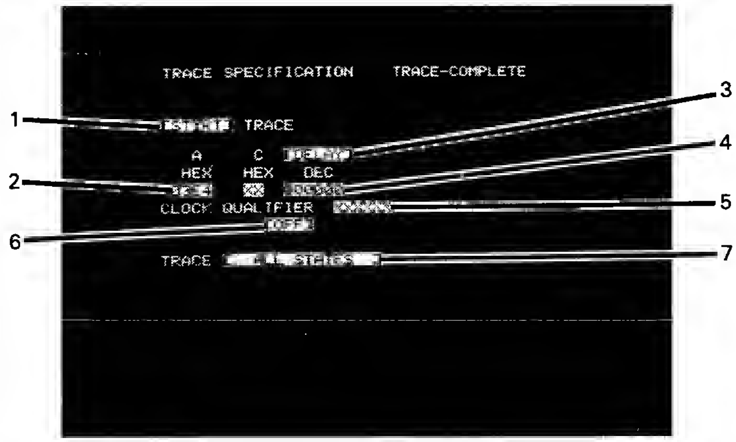
2. **CLOCK SLOPE select:** Move cursor to this field and press FIELD SELECT to use either postive-edge or negative-edge of incoming clock for data acquisition.

3. **LABEL SELECT:** Move cursor to this field and type in the desired label for each probe in the three pods. In the above format specification, the 16 lines of pods 2 and 3 were connected to an address bus and the eight lines of pod 1 were connected to a data bus. This labeling groups the address bus lines under A and data bus under C. Up to three separate groups can be obtained by assignment of A, B, and C labels to the probes. Only adjacent probes can be grouped. The 1615A will not accept a split label assignment such as AAABAACCCC, but by rearranging the label, it will accept AAAAABCCCC or BAAAAACCCC. Assign X to any unused probe to eliminate it from the display and trigger.

4. **LOGIC POLARITY select:** Move cursor to this field and press FIELD SELECT to assign either positive or negative logic polarity to each set of probe inputs.

5. **Number BASE select:** Move cursor to this field and press FIELD SELECT to choose the number base for display of information obtained from each set of probe inputs. Either binary, octal, decimal, or hexadecimal number bases can be selected.

Figure 3-7. 24-bit Format Specification Menu



1. TRACE point select: Move cursor to this field and press FIELD SELECT to place the trigger word at the START or END of the trace. To locate the trigger word within the trace and view activity before and after the trigger, select END TRACE and add some delay as described in steps 3 and 4 below.

2. Trigger Address select: Move cursor to this field and type in the desired trigger words. In the example above, the 1615A will recognize its trigger when the address bus (group A) reaches 03E4 (HEX), regardless of the state on the data bus (group C).

NOTE

The dollar sign ($) may appear in the trigger field. If $ does appear, make sure that the trigger word can be expressed in the selected number base. For example, 1XX0 can be selected as the trigger word when using the binary number base. If the number base is then changed to HEX, $ will appear in the new trigger word. This is because 1XX0 can not be expressed as a unique HEX character.

3. DELAY/OCCUR select: Move cursor to this field and press FIELD SELECT to choose either DELAY or OCCUR. If DELAY is selected, 1615A will count a specified number of clocks after trigger recognition before starting or ending data acquisition. If OCCUR is selected, start or end of data acquisition will be delayed until after a number of trigger occurrences. The number of clocks or trigger occurrences are selected in item 4 below.

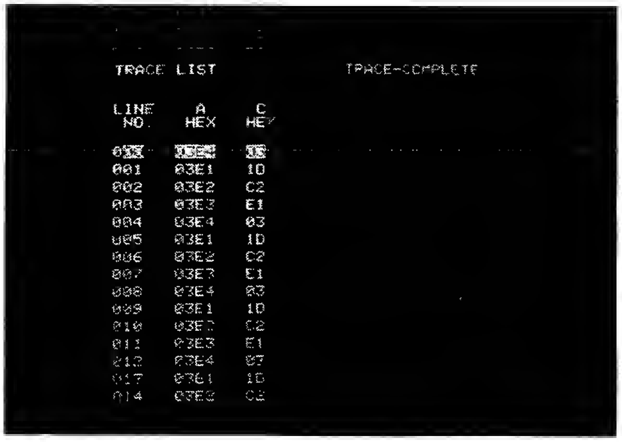
4. DELAY/OCCUR parameter: Move cursor to this field and enter the desired delay (clocks or occurrences). Any delay of clocks or trigger occurrences up to 999 999 can be selected. This parameter is always a decimal number.

5. First CLOCK QUALIFIER word: Move cursor to this field and enter word: 1 or 0 for each of the six qualifier lines used on the clock probe. A "1" requires a high state to qualify the clock. A "0" requires a low state to qualify the clock. Enter X on any qualifier line that is not used.

6. Second CLOCK QUALIFIER word: Move cursor to this field and press FIELD SELECT to either turn OFF the second qualifier word or turn it on to OR it with the first qualifier word. If OR is selected, type in the second qualifier word in the same format as was used for the first qualifier word.

7. TRACE data type: Move cursor to this field and press FIELD SELECT to choose either ALL STATES or TRIGGER EVENTS. If ALL STATES is selected, the 1615A will accept every input received after trigger recognition. If TRIGGER EVENTS is selected, the 1615A will accept only those inputs which are a valid trace specification.

Figure 3-8. 24-bit Trace Specification Menu



This illustrates a typical trace list display. TRACE-COMPLETE in the upper, right-hand corner indicates that the data-acquisition circuitry is now inactive. The trigger word 03E4 appears in inverse video on line 000 (start trace mode). The data acquired by the probes labeled A and C is displayed in separate columns in hexadecimal number bases. To observe other portions of the 256-byte memory, use the ROLL DISPLAY keys on the keyboard. To observe a particular line of display, move the cursor into the LINE NO. column and type in the line number desired. To return to the portion of memory which contains the trigger word, press the AT TRIG WORD key.

Figure 3-9. Trace List Display

3-38. 8-BIT ASYNCHRONOUS TIMING MEASUREMENTS.

3-39. In the 8-bit mode, up to eight lines of asynchronous electrical activity can be monitored through the probes in pod 1. This mode of operation uses the following menus: 8-bit Format Specification (figure 3-21), and 8-bit Trace Specification (figure 3-22). In the 8-bit Format Specification menu, the operator can select the format for display if the optional list is elected. In the 8-bit trace specification menu, the operator selects the area of program execution to be captured using a variety of optional trigger pattern and delay arrangements. Also in this menu, the rate for sampling the eight data lines can be selected either from one of the several internal clock rates, or by supplying a separate external clock through a lead on the clock probe.

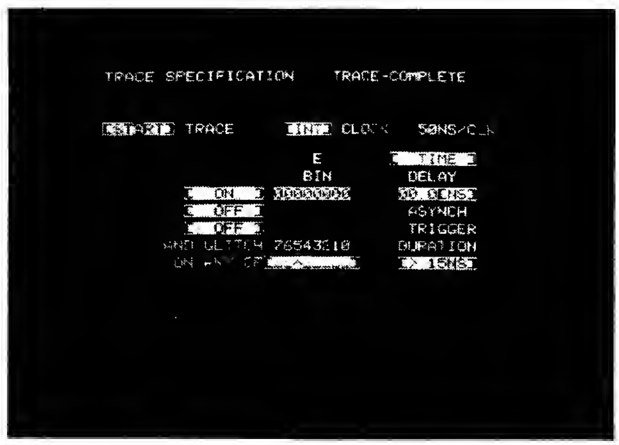


Figure 3-10. Asynchronous Triggering Example

3-40. 8-BIT ASYNCHRONOUS TIMING DIAGRAMS CAPTURE AND DISPLAY. Press the TRACE key. The 1615A will capture 256 bytes of asynchronous, time-related activity and display a timing diagram (figure 3-23) which has one horizontal trace for each active channel. Each trace displays the contents of its 256-bit memory.

3-41. ASYNCHRONOUS TRIGGERING. In figure 3-10, the 1615A has been set up to trigger when it detects that all of the eight input lines have remained low for at least 15 ns and a glitch is detected on line 5 of pod 1. Triggering will be immediate and the trigger point will begin the 256-byte trace.

3-42. In figure 3-11, three OR'd trigger fields are used. The 1615A will trigger whenever it detects a 15-ns period where all eight lines are low, OR all eight lines are high, OR all lines alternate with the first line high and the last line low.

3-43. ON NOT TRIGGERING. This mode of triggering allows the operator to set up a particular status word and then monitor a system. If the status word ever changes, electrical activity before and/or after the change can be captured and analyzed as a timing diagram.

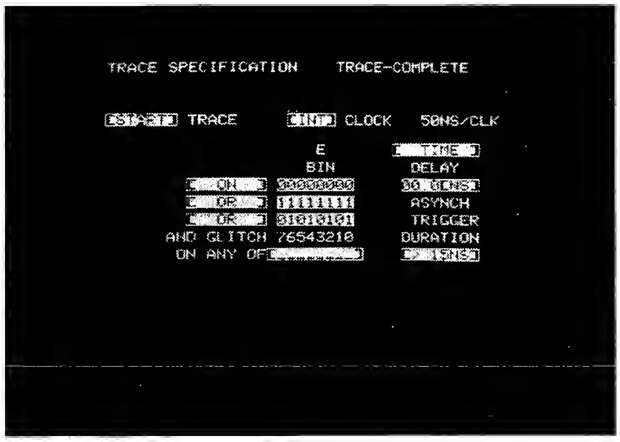


Figure 3-11. Multiple Trigger Words

3-44. ON NOT triggering can also be used to capture a timing diagram of activity leading up to a system crash that stops the system clock. By selecting ON NOT XXXXXXXX, the END TRACE mode, and external clocking, 1615A will gather a continuous flow of activity, and will never find its 8-bit trigger word. When a crash occurs and the clock stops, the timing diagram of activity leading up to the crash will be presented when the STOP key is pressed.

3-45. 8-BIT TRACE DELAYS. The 8-bit trace may be delayed from its trigger point, either by a period of time or by a number of external clocks. In figure 3-12, external clock delay was selected. After the 1615A recognizes that all states on pod 1 are low for 15 ns, it will begin to count clocks applied to the EXT clock input of the clock probe. When it counts 142 external clocks, it will then gather 256 bytes of data at the rate of the internal clock (50 ns/clock in figure 3-12). The DELAY QUALIFIER field could have been used. The qualifier lines of the clock probe could have been connected to a particular set of lines and entrys made to ensure that only those external clocks which arrived when certain states were true would be recognized as part of the delay specification. For example, data collection could have been delayed until after a specific number of I/O writes had occurred.

Figure 3-12. 8-bit Trace Delays

3-46. RELATIVE TIME MEASUREMENTS. Figure 3-13 demonstrates the process for making relative time measurements on a timing diagram. In section a, the ROLL DISPLAY keys were used to place the leading edge of the expand indicator (brightened trace segment) on the falling edge of a pulse on line 0. Then the FIELD SELECT key was pressed to zero the measurement indicator. In section b, the expand indicator was moved to the falling edge of a pulse on line 1. The measurement indicator shows that there is an elapsed time of 11.8 usec between the two points of interest.

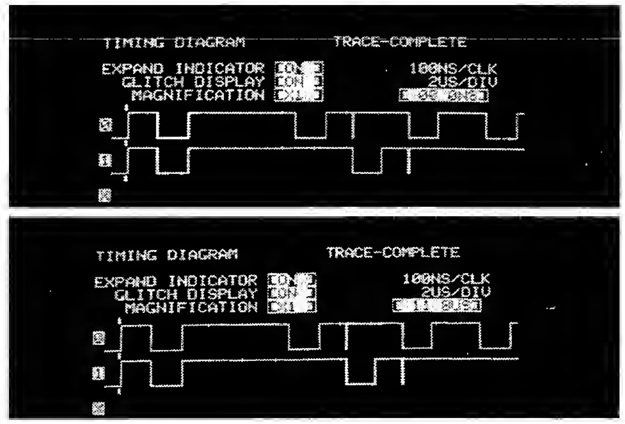


Figure 3-13. Relative Time Measurements

3-47. For ease of making timing measurements, the channels can be rearranged on the display. In figure 3-14, channels 0 and 7 were placed next to each other. To rearrange channels, move the cursor into the channel number column and type in the desired order of channel numbers. To return the channels to the normal sequence of presentation, press the CHAN SEQ key.

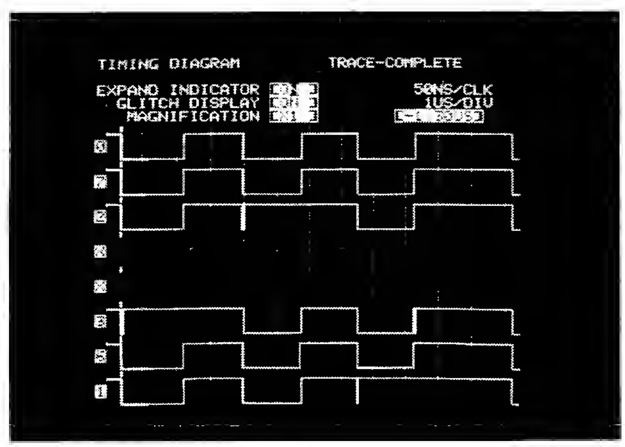


Figure 3-14. Rearranged Channel Sequence Displays

3-48. POSITIVE/NEGATIVE TIME ON TIMING DIAGRAM. The 1615A can be set up to capture and display a timing diagram showing activity leading up to the trigger pattern, the trigger point itself, and activity following the trigger pattern. In figure 3-15, the 8-bit mode was set up for the trigger pattern to end the trace. Then delay was added to the trace specification so that an additional portion of activity would be captured following recognition of the trigger pattern.

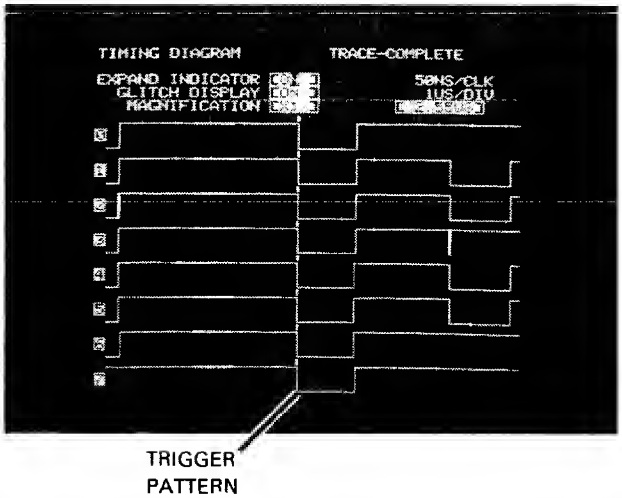


Figure 3-15. Positive/Negative Time Displays

3-49. TRACE LIST/TIMING DIAGRAM CONVERSION. The 1615A provides the capability of converting a timing diagram to a trace list and a trace list to a timing diagram. In this way, activity gathered by pod 1 in either mode of operation can be viewed both as a series of sequential states, and as a 256-byte trace. (See figure 3-16.)

3-50. GLITCHES. A glitch is defined as two or more transitions occurring between any two consecutive samples. When a glitch is detected by the 1615A, an intensified vertical line is shown on the 1615A display in the time frame where the glitch detection occurred. Figures 3-17 through 3-19 will clarify the 1615A glitch detection and display.

3-51. Figure 3-17 shows detection and display of a single glitch occurring between two consecutive samples. The data level crosses the threshold twice between T1 and T2, and the 1615A displays an intense vertical bar at T2.

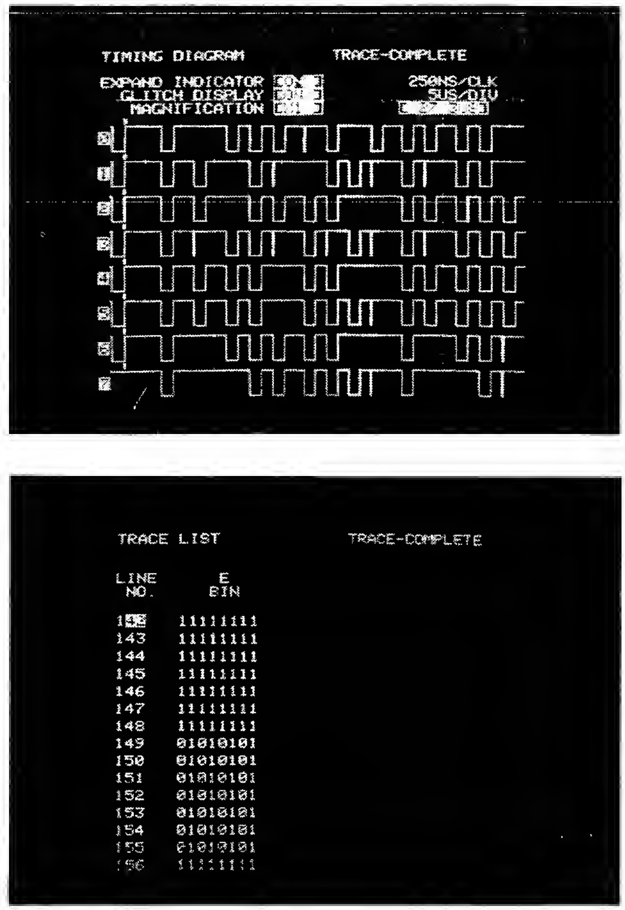


Figure 3-16. Trace List/Timing Diagram Conversion

3-52. Figure 3-18 shows detection and display of a glitch occurrence between T1 and T2 (two or more transitions crossed the threshold between T1 and T2). The 1615A can not detect and display more than one glitch between any two consecutive samples. If in doubt, a faster clock rate can be selected to detect glitches.

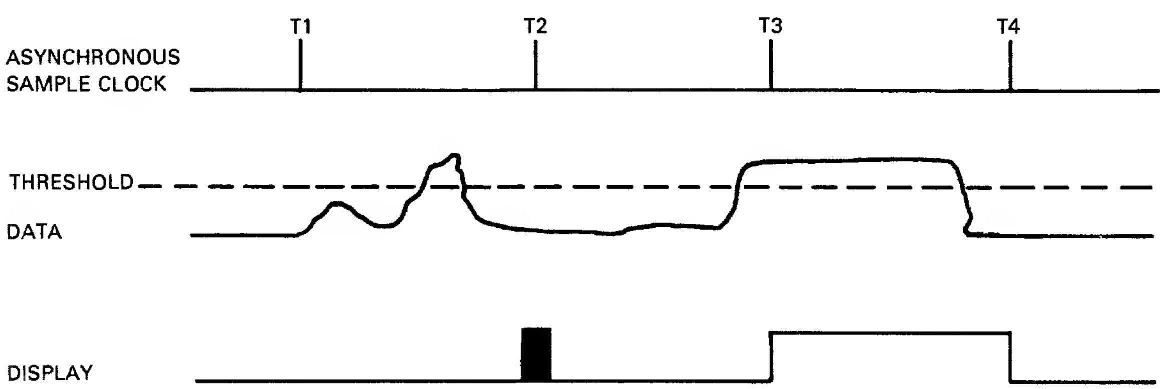


Figure 3-17. Single Glitch Detection and Display

3-53. Figure 3-19 shows detection and display of a glitch that occurred within the same sample period as a data transition. The glitch is displayed as an intensified data transition.

3-54. Figure 3-20 shows an example which includes glitch detection as part (or all) of the asynchronous trigger specification. In the example, the trigger word is all 1's on the eight asynchronous data channels plus detection of a glitch on either bit 3 or bit 7. It was not necessary to detect glitches on both bits 3 and 7. The entire glitch trigger field is satisfied whenever a glitch is found in any one of the designated bits. In the illustration, no trigger would have been recognized if only bits 0 through 6 had been designated since the glitch occurred on bit 7.

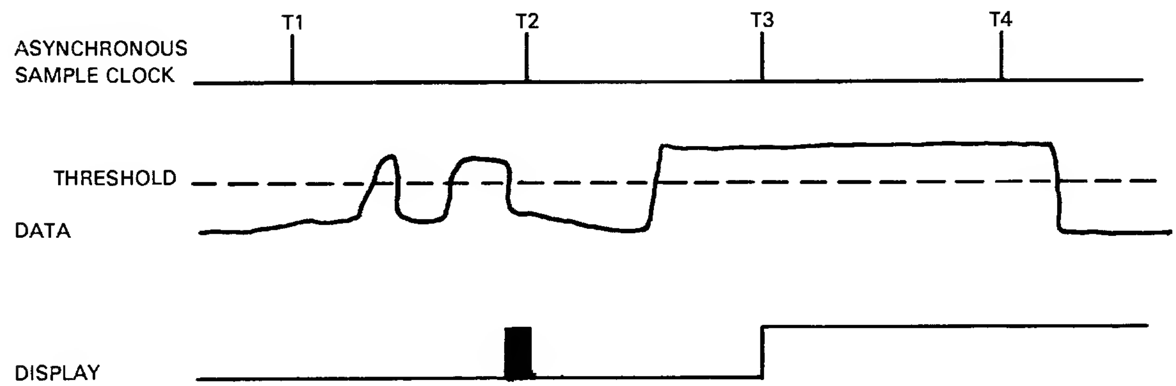


Figure 3-18. Multiple Glitch Detection and Display

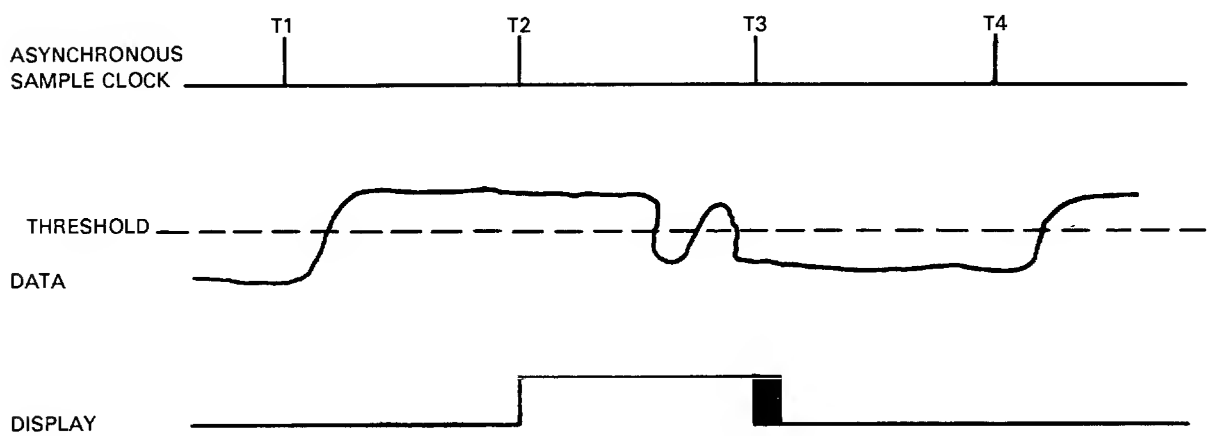


Figure 3-19. Glitch Detection and Data Transition Display

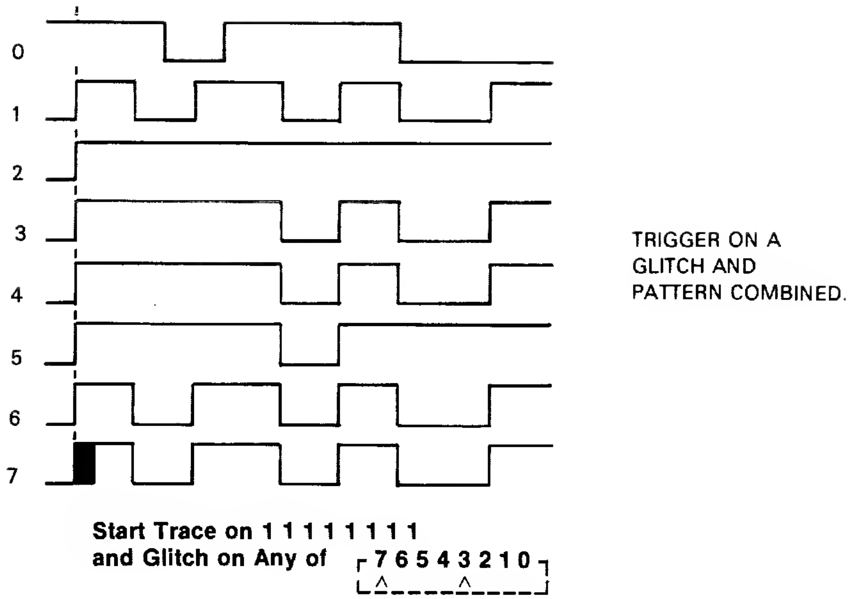
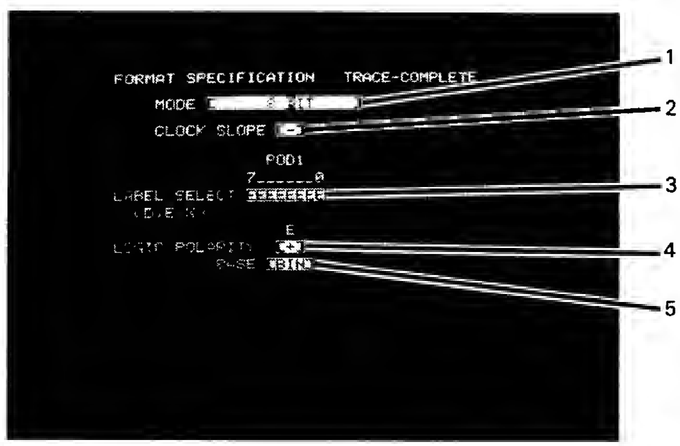
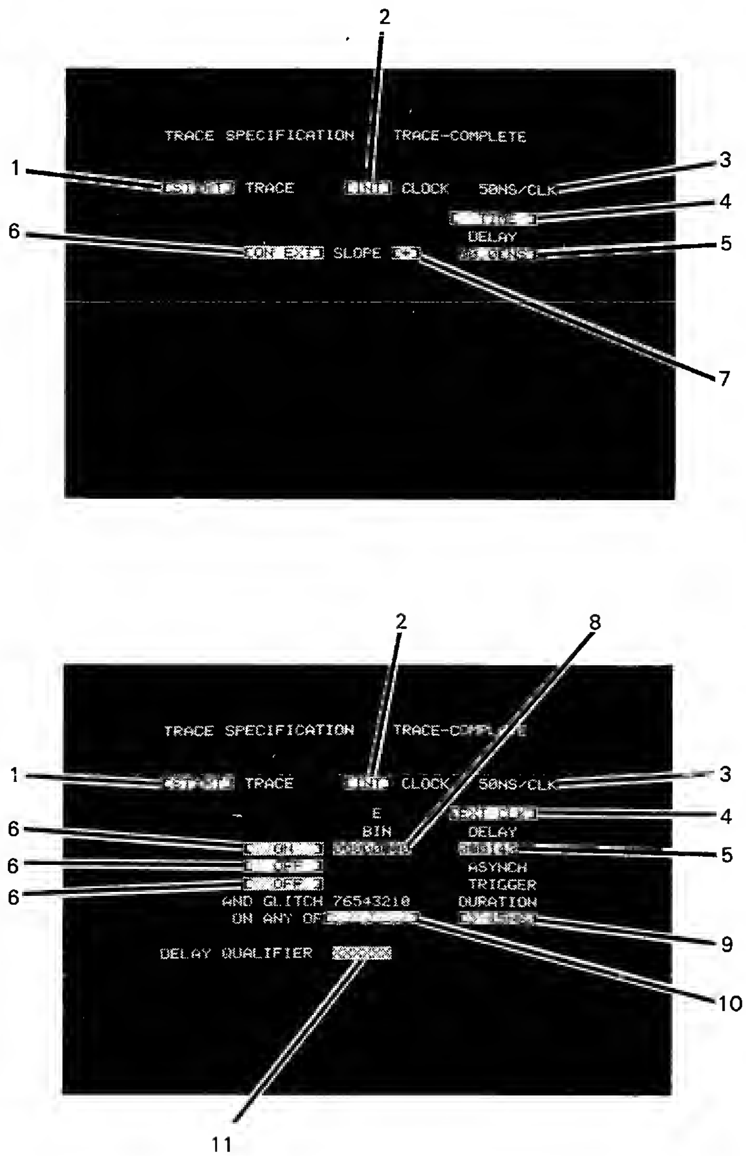


Figure 3-20. Trigger on Combined Pattern and Glitch



1. **MODE select:**	Move cursor to this field and press FIELD SELECT key to obtain 8 BIT mode.
2. **CLOCK SLOPE select:**	Move cursor to this field and press FIELD SELECT to use either positive-edge or negative-edge of incoming clock for data acquisition.
3. **LABEL SELECT:**	Move cursor to this field and type in the desired label for each probe in pod 1. The probes can be arranged in one or two groups for a list presentation by labeling some probes D and others E. Only adjacent probes can be grouped. The 1615A will not accept DDEEDDEE. Label unused probe channels with X to eliminate them from the display and trigger.
4. **LOGIC POLARITY select:**	Move cursor to this field and press FIELD SELECT to assign either positive or negative logic polarity to each set of probe inputs.
5. **Number BASE select:**	Move cursor to this field and press FIELD SELECT to choose the number base for a list display of information obtained from each set of probe inputs. Either binary, octal, decimal, or hexadecimal number bases may be selected.

Figure 3-21. 8-bit Format Specification Menu



1. **TRACE point select:** Move cursor to this field and press FIELD SELECT to place the trigger word at the START or END of the trace. To locate the trigger within the trace and view activity before and after the trigger, select END trace and add some delay as described in steps 4 and 5 below.

2. **Clock Source select:** Move cursor to this field and press FIELD SELECT to choose either the internal clock or an external clock for developing a timing diagram.

3. **Sample Period select:** The cursor is not used to access this field. Press the SAMPLING RATE keys on the keyboard to increment (INCR) or decrement (DECR) the sample period. Twenty-two sample periods are available from 50 NS/CLK to 500 MS/CLK.

4. **Delay Type select:** Move cursor to this field and press FIELD SELECT to choose either TIME delay, or delay by a number of external clocks (EXT CLK).

Figure 3-22. 8-bit Trace Specification Menu

5. **Delay Parameter select:** Move cursor into this field and type in the desired trigger delay: either a time period or number of external clocks. Delay up to 1 048 575 sample clocks can be selected. Any time delay may be entered. The 1615A will automatically round off the time delay to a multiple of the sample period selected in step 3.

6. **Trigger Status select:** Move cursor into this field and press FIELD SELECT to choose the desired trigger status. ON sets the 1615A to trigger when it detects the adjacent word. ON NOT sets the 1615A to trigger on anything but the adjacent word. ON EXT sets the 1615A to trigger when the selected transition occurs on the external trigger line of the clock pod (see step 7).

7. **External Trigger SLOPE select:** Move cursor into the field and use FIELD SELECT to choose either positive-edge or negative-edge triggering for the external trigger line from the clock pod.

8. **Trigger Word select:** Move cursor into this field and type in the desired trigger word. The entry must be in the number base specified for the label field. In the example, all probe leads were combined in group E and binary number base was selected so only 1, 0, or X are allowed values for this entry.

NOTE

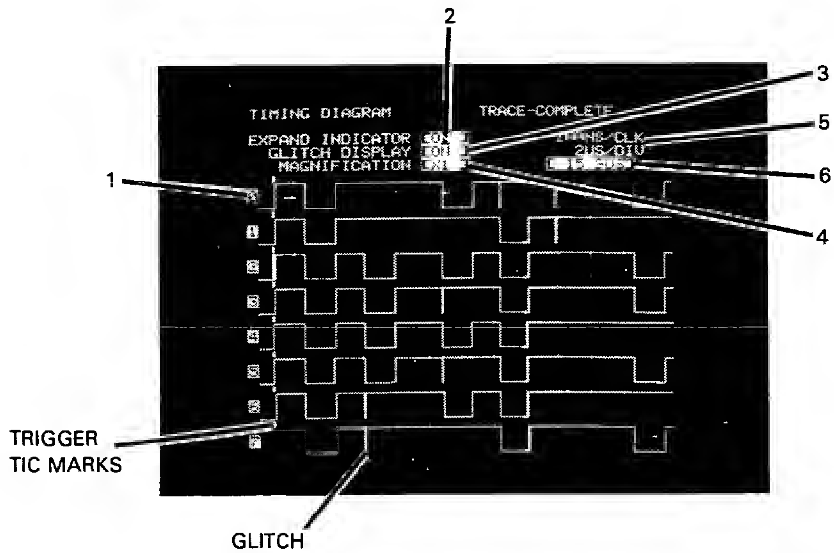
The dollar sign ($) may appear in the trigger field. If $ does appear, make sure that the trigger word can be expressed in the selected number base. For example, 1XX0 can be selected as the trigger word when using the binary number base. If the number base is then changed to HEX, $ will appear in the new trigger word. This is because 1XX0 can not be expressed as a unique HEX character.

9. **ASYNCH TRIGGER DURATION select** Move cursor into this field and press FIELD SELECT to choose the period of time that the trigger set must remain stable before it is recognized as a valid 1615A trigger word.

10. **GLITCH trigger select:** Move cursor into this field and press FIELD SELECT to assign glitch requirements to the trigger specification, if desired. A peak under a channel number assigns a glitch trigger requirement to that channel. This field is satisfied when any one of the specified channels detects a glitch.

11. **DELAY QUALIFIER select:** Move cursor to this field and enter qualifier states desired for the clock probe. Use 1 (high state qualifies), 0 (low state qualifies), or X (either state qualifies). DELAY QUALIFIER is only available when external clock delay is selected. This field allows the operator to establish a qualification requirement for the clocks that are counted as part of the delay.

Figure 3-22. 8-bit Trace Specification Menu (Cont'd)



1. **CHANNEL SEQUENCE select:** Move cursor into this field and type in desired order of channel presentation. This allows placing any desired channels side-by-side for comparisons. Use letter X to blank a channel slot on the CRT.

2. **EXPAND INDICATOR select:** Move cursor into this field and press FIELD SELECT to turn ON or OFF the expand indicator. This 1-division brightened portion of the trace is the area that will be displayed on screen if X10 MAGNIFICATION is selected. It can be positioned anywhere on the display by using the ROLL DISPLAY keys. It may mask glitch display so it can be turned off if desired.

3. **GLITCH DISPLAY select:** Move cursor into this field and press FIELD SELECT to turn ON or OFF the display of glitches. This can reduce display clutter when making timing measurements.

4. **MAGNIFICATION select:** Move cursor into this field and press FIELD SELECT to choose either X1 or X10 display magnification. A 1-division brightened portion of the display in X1 magnification shows what part of the trace will be on screen in X10 magnification.

5. **Sample period/Horizontal Time Scale:** Use SAMPLE PERIOD INCR/DECR keys to change internal clock rate for next trace. After incrementing or decrementing the sample period, the horizontal scale indications will be invalid for the displayed data until a new trace is obtained.

6. **Time Measurement Field:** Move cursor to this field and press FIELD SELECT key to zero indications. Then use ROLL DISPLAY keys to move expand indicator along trace. Time measurement field will show the elapsed time between the present and original position of the expand indicator.

Figure 3-23. Timing Diagram Display

3-55. SIMULTANEOUS SYNCHRONOUS/ ASYNCHRONOUS MEASUREMENTS.

3-56. The 1615A offers a dual mode of operation where the 16 bits gathered by pods 2 and 3 are clocked in for state analysis and the 8 bits gathered in pod 1 are captured asynchronously for timing analysis. This mode is used when the area of concern involves both synchronous and asynchronous activity, such as finding the source of glitches at a particular point in program execution. The dual mode gathers its information via one of four interactive trigger modes (see ARMS/TRIGGERS paragraph).

3-57. In the Format Specification menu (figure 3-26), the operator sets up the individual formats for the 16-bit and 8-bit analyzers. In the Trace Specification menu (figure 3-27), the synchronous and asynchronous trigger and delay specifications are established for each of the two separate functions. Both menus offer nearly the same parameters as are offered for the 24-bit and 8-bit modes, except that only one qualifier field is available for the state analyzer and the Trigger Events mode is not used.

3-58. ARMS/TRIGGERS. Two modes of interactive operation (ARMS and TRIGGERS) are available when the 1615A is simultaneously used as a 16-bit synchronous state analyzer and an 8-bit asynchronous timing analyzer. The effects of the two modes are shown in figures 3-24 and 3-25.

3-59. 16 BIT TRIGGERS 8 BIT (figure 3-24). In this mode, the state analyzer receives external clocks while the timing analyzer waits. With each external clock, the 16-bit state analyzer examines the associated data word. When the state analyzer recognizes its trigger word, it starts to retain data bytes in the 16-bit state memory according to the mode of operaton selected. At the same time that the state machine recognizes its trigger, it issues a trigger to start the 8-bit timing analyzer. The timing analyzer then gathers 256 8-bit bytes into its timing memory. Since the two analyzers operate independently, they may gather data at different clock rates, as shown in figure 3-24. This enables an operator to obtain a timing diagram of the activity associated with a very small portion of an operating program.

3-60. By using the TRIGGERS mode of triggering, the following applications are available:

a. Lines can be observed to detect the source of a false interrupt (asynchronous condition) which occurs at a particular point in program execution (synchronous state).

b. The stability of input lines can be verified (asynchronous activity) prior to reading an I/O port (synchronous state).

c. Control line states (asynchronous activity) can be checked during a subroutine call (synchronous state).

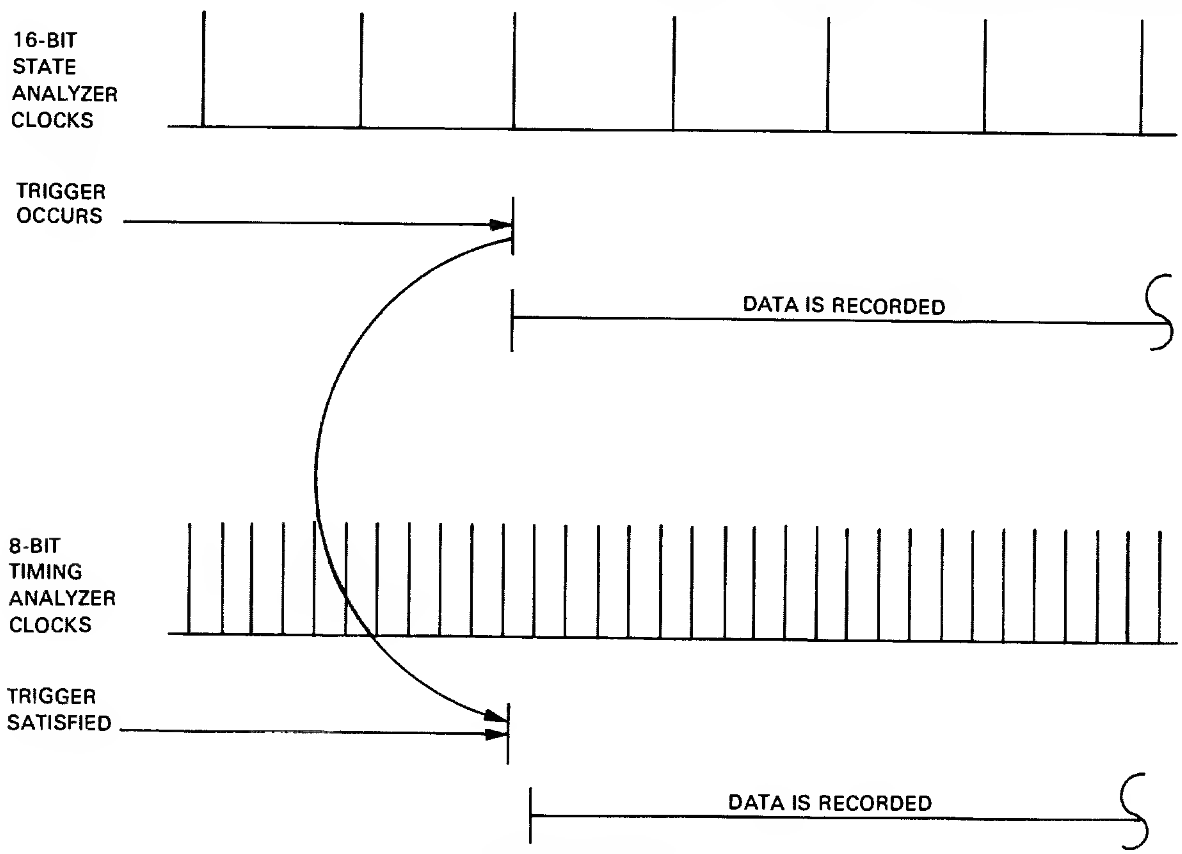


Figure 3-24. 16 BIT TRIGGERS 8 BIT Mode

3-61. 16 BIT ARMS 8 BIT (figure 3-25). In this mode, each of the two analyzers search for their own unique trigger words. The state analyzer starts searching for its trigger word as soon as the run begins, but the timing analyzer is held in a disarmed mode. When the state analyzer finds its trigger, it arms the timing analyzer, allowing it to start its own trigger word search. When the timing analyzer finds its trigger word, it then acquires its 256 bytes of data. In this mode, both digital and time delay can be obtained in one measurement.

3-62. By using the ARMS mode of operation, the 1615A can be set up to search for a particular pattern on a set of control lines (asynchronous acitivity) only after a specific point in program execution (synchronous state). One application of this mode would be to monitor a status word for change (asynchronous activity) after completion of a bootstrap (synchronous state).

3-63. The 1615A also offers the 8 BIT TRIGGERS 16 BIT and 8 BIT ARMS 16 BIT modes of triggering. These modes are identical to those described above, except that the 8-bit timing analyzer begins watching the incoming data at the start of the run and the 16-bit state analyzer waits to receive an enable or trigger.

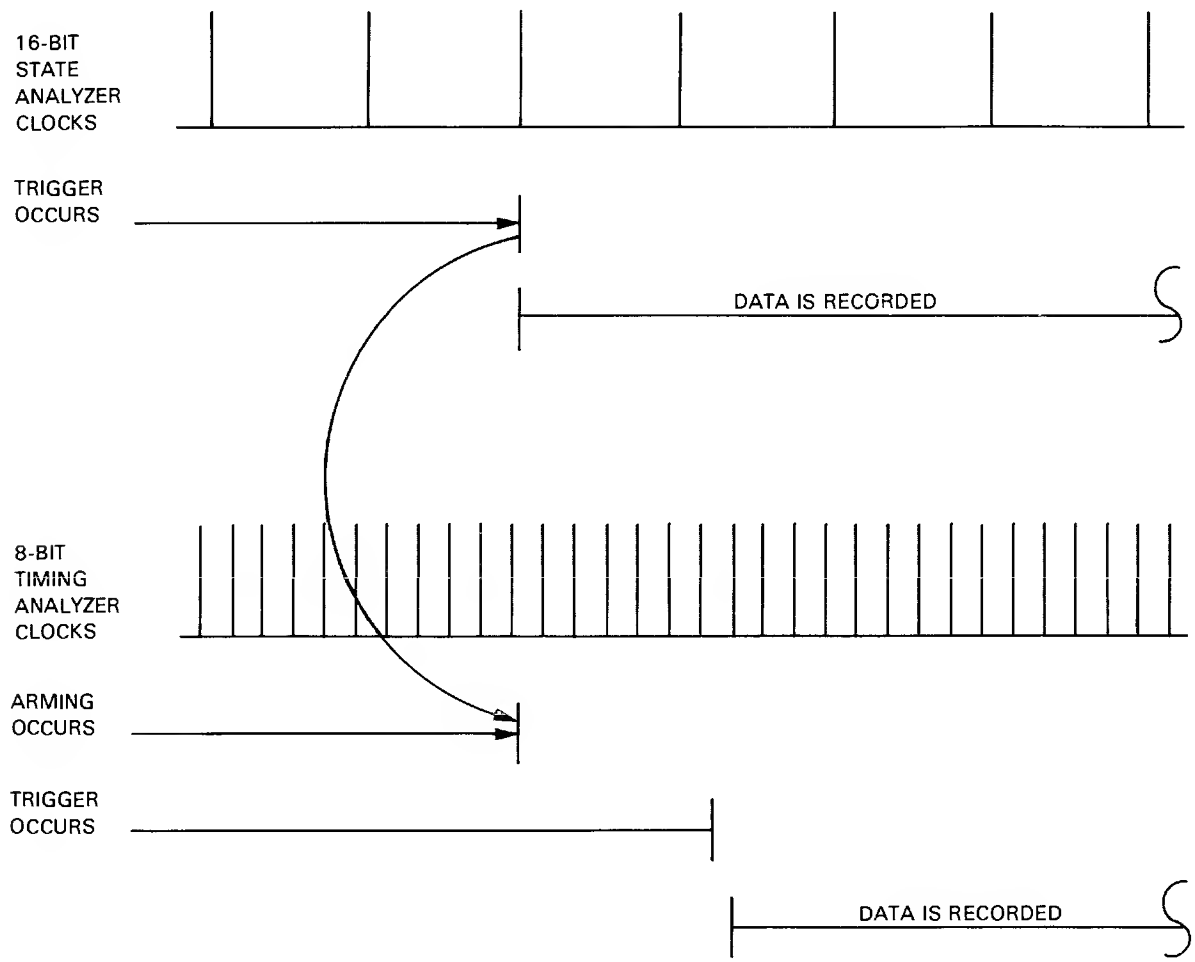
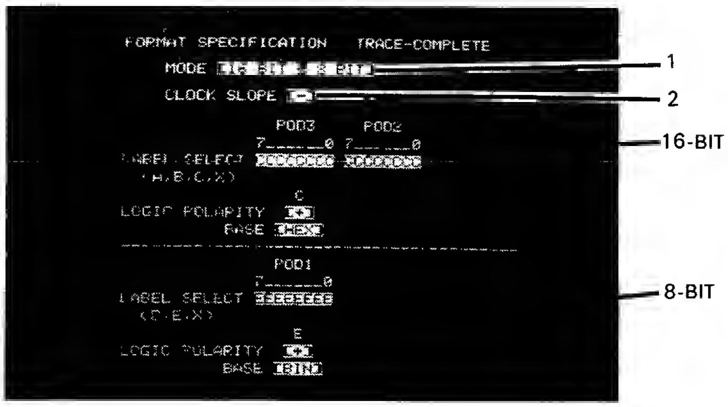


Figure 3-25. 16 BIT ARMS 8 BIT Mode



1. MODE select: Move cursor into this field and press FIELD SELECT to obtain 16 and 8 BIT MODE.

2. CLOCK SLOPE select: Move cursor to this field and press FIELD SELECT to use either positive- edge or negative-edge of incoming clock for data acquisition.

The 16-bit format specification menu is shown above the dashed horizontal line on the display. Menu selections are made in the same manner as for the 24-BIT FORMAT SPECIFICATION, except that only the 16 probes of pods 2 and 3 are available for synchronous state measurement.

The 8-bit format specification menu is shown below the dashed horizontal line on the display. Menu selections are made in the same manner as for the 8-BIT FORMAT SPECIFICATION.

Figure 3-26. 16-bit & 8-bit Format Specification Menu

1. Trigger Interaction select: Move cursor to this field and press FIELD SELECT to choose one of the four trigger interaction modes:
(1) 16 BIT ARMS 8 BIT
(2) 16 BIT TRIGGERS 8 BIT
(3) 8 BIT ARMS 16 BIT
(4) 8 BIT TRIGGERS 18 BIT

The 16-bit trace specification menu is shown above the dashed horizontal line on the display. Menu selections are made in the same manner as for the 24 BIT TRACE SPECIFICATION, except that only one CLOCK QUALIFIER field is available and the TRIGGER EVENTS mode is eliminated.

The 8-bit trace specification menu is shown below the dashed line on the display. Menu selections are made in the same manner as for the 8-BIT TRACE SPECIFICATION.

Figure 3-27. 16-bit & 8-bit Trace Specification Menu

3-64. STATUS MESSAGES.

3-65. The following messages are displayed on the 1615A screen to provide an indication of 1615A operating status. (Messages may vary with different 1615A options.)

COMMAND IGNORED - Displayed when an error exists in the operator's entry.

DELAY OUT OF RANGE - Displayed when delay specification exceeds 1615A capabilities.

ERROR IN RAM # - Displayed when 1615A detects a write and read-back error during the power-up self test.

ERROR IN ROM # - Displayed when 1615A detects a check-sum failure during power-up self test.

INVALID ENTRY - Displayed when an entry is made that does not fit the field definition, such as entering an 8 in an octal field.

NO ASSIGNED LABEL - Displayed when all probes are labeled X, an invalid condition.

NO TRIGGER - Displayed between the time that the 1615A starts looking for its trigger and the time that it finds its trigger.

NO 16 BIT TRIGGER - Displayed between the time that the 1615A starts looking for its 16-bit trigger and the time that it finds its trigger.

NO 8 BIT TRIGGER - Displayed between the time that the 1615A starts looking for its 8-bit trigger and the time that it finds its trigger.

POWER UP COMPLETE - Displayed after the end of the self test if the self test detected proper operation.

POWER UP FAILED - Displayed after the end of the self test if the self test detected improper operation.

SLOW CLOCK - Displayed when the repetition rate of the external clock is slow.

SPLIT LABEL - Displayed when the letter assignments in the probe label field are not contiguous.

TEST COMPLETE - Displayed when the data-acquisition self test is completed and the 1615A is found to be operating properly.

TEST FAILED, STATUS – - Displayed when an error is detected during the data-acquisition self test. Interpretation of status codes is further explained in Section VIII of this manual.

TEST IN PROCESS - Displayed during the time that the 1615A is performing a self test.

TRIGGER NOT IN MEMORY - Displayed when the AT TRIG WORD key is pressed and the trigger word is not in memory, due to trigger delays, etc.

UNALLOWED VALUE - Displayed only in decimal fields when an out-of-range entry is made.

USE FIELD SELECT KEY - Displayed when the operator presses one of the alphanumeric keys in a field that is controlled by the FIELD SELECT key.

>0<256 WDS - Displayed only when operating with a slow external clock capturing state data in the trigger starts trace mode. This message tells how many valid data words have been captured since the start of the trace, and before the trace is complete.

3-66. OPERATOR'S TESTS.

3-67. Several test routines have been built into the 1615A. These routines are available to the instrument operator through front-panel selection. Each test provides a simple method of ensuring reliability in the specific function or functions tested. If a self-test failure occurs, be sure to check all external connections.

3-68. POWER-UP SELF TEST.

3-69. This self test is performed automatically at instrument turn on if no keyboard key is held down. Built-in routines check the instrument program ROMs, display RAM for alphanumeric displays, and the microprocessor RAM. Successful completion of this test is indicated when the CRT displays the 24-bit format specification with POWER UP COMPLETE in the upper, right-hand corner. A failure in this test sets the test in a loop and the CRT indicates the circuitry that failed, such as ERROR IN ROM #3, 4, 5. The 1615A continues to rerun the test and refresh the display. When the malfunction is corrected, the 1615A will proceed through the remainder of the power-up test and finish with POWER UP COMPLETE and the 24-bit format specification.

3-70. KEYBOARD SELF TEST.

3-71. The keyboard self test is initiated when the A key is held down during instrument turn on. In this test, the display shows NEXT KEY #1, LAST KEY #13. To individually check the proper operation of the entire keyboard, the keys must be pressed in sequence from left to right and top to bottom in each functional group. The LAST KEY # will show the number of the last key pressed but the NEXT KEY # will only advance if the next key specified is pressed. To end this test, press the STOP key. Then the display will switch to the 24-bit format specification.

3-72. If a key (other than A through D) is stuck down during power up, the display will show POWER UP FAILED, and LAST KEY # will show the number of the stuck key.

3-73. DATA ACQUISITION SELF TEST.

3-74. The data acquisition self test is initiated when the B key is held down during instrument turn on. A program of test data is begun which exercises all variables in the data acquisition circuitry. The clock probe must be connected to the SELF-TEST CLOCK and COMMON test points on the front panel to perform this test. At the end of the test, the display shows the 24-bit format specification menu and TEST COMPLETE in the upper, right-hand corner.

3-75. If a failure occurs during the data acquisition test, the display will show TEST FAILED, STATUS = (code number). The code number is always in octal and indicates machine status at the time of the failure. Refer to Section VIII of this manual for a list of failure codes and their interpretations.

3-76. Press FORMAT SPECIFICATION and TRACE SPECIFICATION; the display will show what state of the test was in process when the failure occurred. When the cause of the failure is discovered and corrected, the test that failed can be repeated by pressing the TRACE key. However, the untried remaining tests in the data acquisition self test will not be performed. To perform the entire data acquisition self test, turn off instrument power and turn it back on while holding the B key down.

3-77. Section VIII contains a list of the tests performed during the data acquisition self test. By referring to Section VIII, you can determine which portions of the circuitry were found to be operating properly, which portion of the circuitry failed the test, and which portions of the circuitry were not tested.

3-78. If you do not wish to perform the remainder of the data acquisition self test, press the TRACE SPECIFICATION key and make a change to the displayed trace specification. This removes the internal count-up mode from the input circuitry and reconfigures the 1615A to acquire external data.

3-79. DSA TEST LOOPS.

3-80. While these functions are not truly instrument self tests, they are included here because they are conditions accessible from the front panel. Each test condition configures its related circuitry in a loop for troubleshooting with DSA measurements. In both of these conditions, the keyboard is disabled. To terminate either of these conditions, instrument power must be turned off.

3-81. DATA ACQUISITION DSA MEASUREMENTS CLOCK. This clock is initiated when the C key is held down during instrument turn on. In this condition, TEST IN PROCESS is displayed on screen and a clock is supplied to the SELF-TEST CLOCK terminal for use in troubleshooting the data acquisition circuits.

3-82. DISPLAY DSA MEASUREMENTS. The display DSA measurements mode is initiated when the D key is held down during instrument turn on. The clock probe must be connected to the SELF-TEST CLOCK and COMMON test points on the 1615A front panel. In this mode, the keyboard is disabled and the display shows a timing disgram of the clock with each probe channel running at one-half the rate of the channel above it. In this mode, the microprocessor is halted and the circuitry is configured in a loop which can be used for DSA testing of the display logic circuits.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section test the instrument electrical performance using the specifications of table 1-1 as the performance standards. All tests can be performed without access to the interior of the instrument. A simpler operational test is included in Section III under Operator's Tests.

4-3. EQUIPMENT REQUIRED.

4-4. Equipment required for the performance tests is listed in the Recommended Test Equipment table in Section I. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model(s).

4-5. TEST CONNECTOR.

4-6. The performance tests and adjustment procedures require connecting pulse generator outputs to probe pod inputs. These tests require either one or two 50-ohm terminations. Figure 4-1 shows how to build a connector that includes a 50-ohm termination for a pulse generator. The Hewlett-Packard part numbers for the parts used in the test connector are listed below. Equivalent parts may be used.

BNC connector	1250-0083
solder lug	0360-1632
nut	2950-0001
2 resistors, 1 watt, 100 ohms	0760-0024

4-7. TEST RECORD.

4-8. The results of the performance tests may be tabulated on the Test Record at the end of the procedures. The Test Record lists all the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for later comparisons during periodic maintenance, troubleshooting, and after repairs or adjustments.

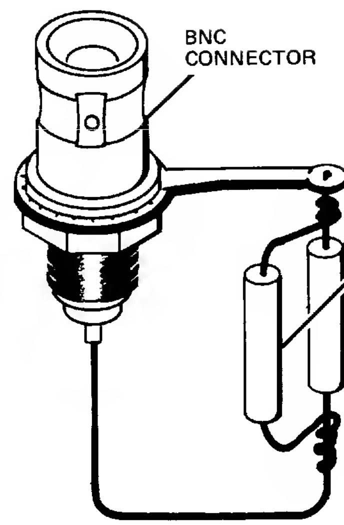


Figure 4-1. 50-ohm Test Connector

4-9. OPERATION VERIFICATION.

4-10. To assure that the 1615A is operating properly without testing all of the specifications listed in table 1-1, perform the Operator's Tests described in Section III of this manual. Make certain that each of the self tests can be accessed via the applicable keyboard keys and that each test reaches its designed conclusion. This verifies proper instrument operation.

4-11. SPECIFICATIONS TESTS.

4-12. The following tests verify the specifications listed in table 1-1. They can be used as an incoming inspection procedure, or for performance testing after instrument repairs or adjustments have been made.

PERFORMANCE TESTS

4-13. CLOCK, QUALIFIER, AND DATA INPUTS TEST.

SPECIFICATION:

REPETITION RATE: to 20 MHz.
MINIMUM INPUT:
Swing 0.6 V.
Clock Pulse Width: 20 ns at threshold level.
Setup Time: time data must be present prior to clock transition, 20 ns.
Hold Time: time data must be present after clock transition, zero.
INPUT THRESHOLD: TTL, fixed at approx. +1.5 V; variable ±10 Vdc.
INPUT RC: 50 kΩ shunted by ⩽14 pF at probe tip.

DESCRIPTION:

This test verifies the specifications of the 10248B input probes when used with the 1615A Logic Analyzer. Each data probe should be tested separately.

EQUIPMENT:

Pulse Generators (2)
Oscilloscope
Multimeter
LCR Meter

PROCEDURE:

a. Connect pulse generators and oscilloscope to 1615A as shown in figure 4-2. Connect all inputs of clock probe and probe pod 1 to their respective signal sources. Connect probe pods 2 and 3 to Model 1615A but do not apply signals to these probe pods.

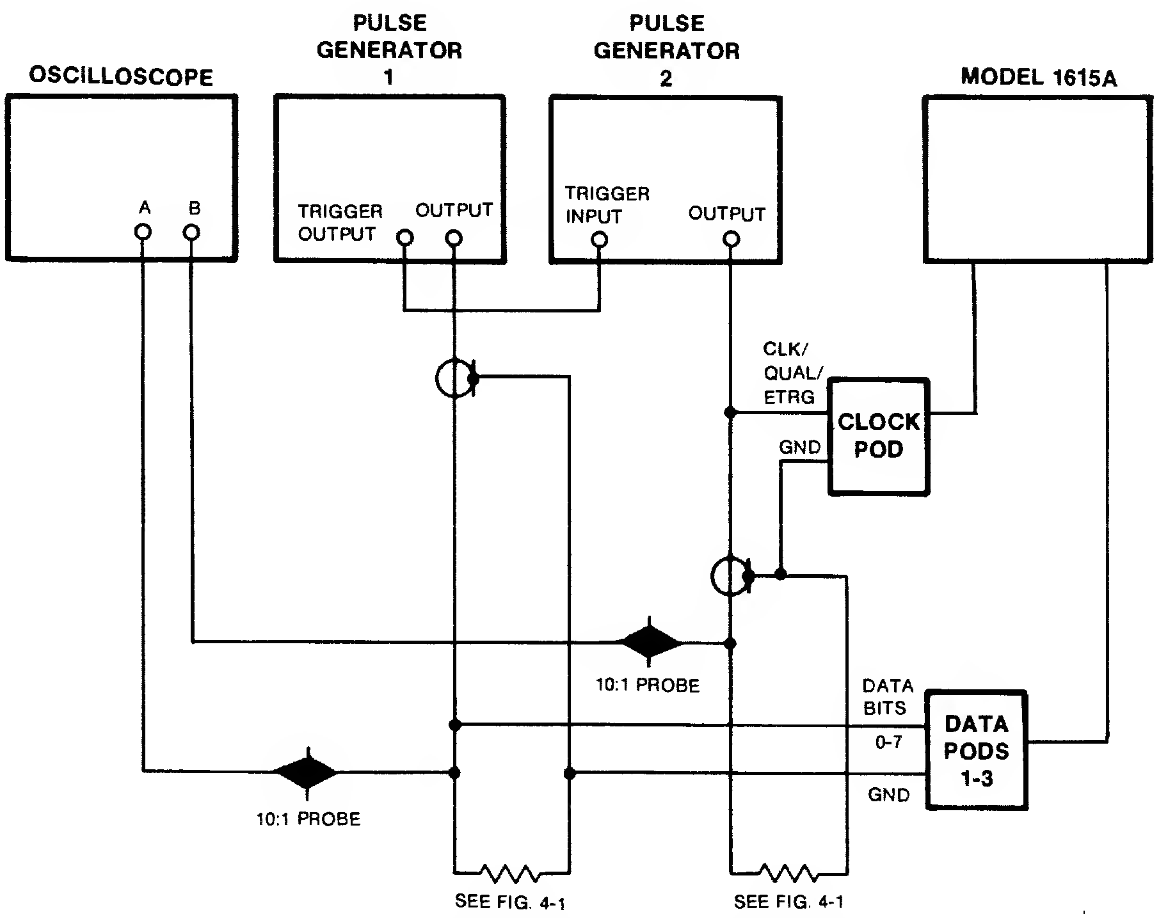


Figure 4-2. Clock, Qualifier, and Data Inputs Test Setup

PERFORMANCE TESTS

b. Set up pulse generators to supply waveforms shown in figure 4-3.

c. Press FORMAT SPECIFICATION key on 1615A.

d. Use CURSOR keys to move cursor to each field in menu. Set up menu according to figure 4-4.

e. Press TRACE SPECIFICATION key.

f. Use CURSOR keys to move cursor to each field in menu. Set up menu according to figure 4-5.

g. Set each PROBE THRESHOLD LEVEL switch to TTL.

h. Press TRACE key. Observe trace list of FF on probe pod 1 and ØØ on pods 2 and 3.

i. Remove inputs from probe pod 1 and connect to probe pod 2.

j. Press TRACE key. Observe trace list of FF on probe pod 2 and ØØ on pods 1 and 3.

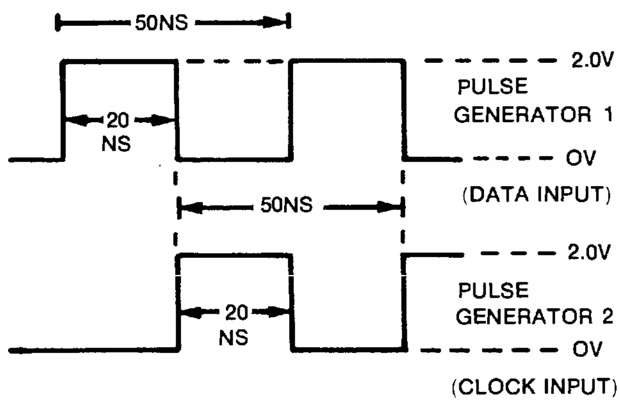


Figure 4-3. Clock, Qualifier, and Data Inputs Test Waveform

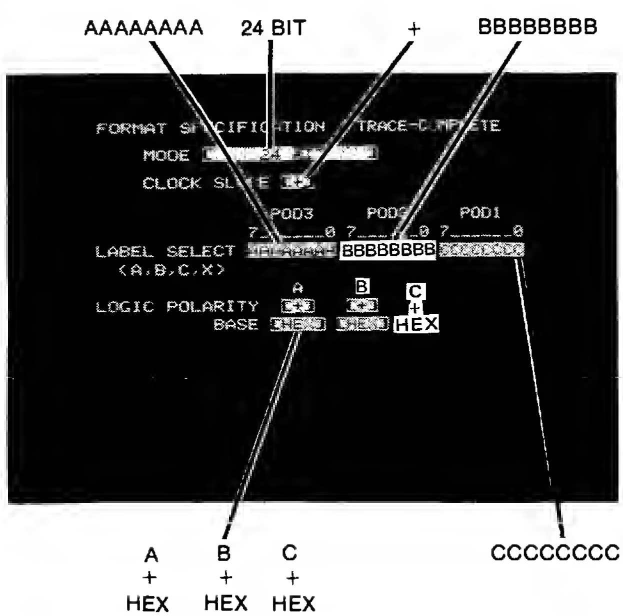


Figure 4-4. Format Specification for Clock, Qualifier, and Data Inputs Tests

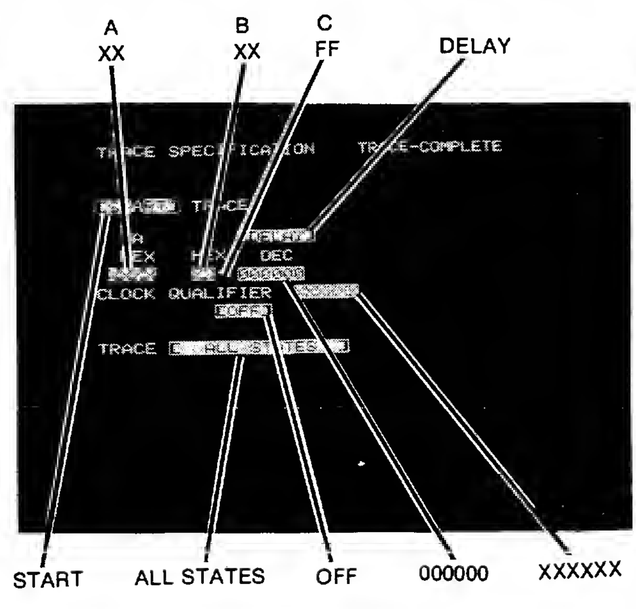


Figure 4-5. Trace Specification for Clock, Qualifier, and Data Inputs Tests

PERFORMANCE TESTS

k. Remove inputs from probe pod 2 and connect to probe pod 3.

l. Press TRACE key. Observe trace list of FF on probe pod 3 and ØØ on pods 1 and 2. This verifies the 1615A specifications as follows:
   REPETITION RATE: to 20 MHz.
   MINIMUM INPUT
   Clock Pulse Width: 20 ns at threshold level.
   Setup Time: 20 ns.
   Hold Time: zero.

m. Connect multimeter to each MEASURE test point on PROBE THRESHOLD LEVEL panel. Multimeter should indicate approximately +1.5 Vdc (TTL threshold).

n. Set PROBE THRESHOLD LEVEL switches to VARIABLE and recheck each MEASURE test point with multimeter. Turn each ADJUST control throughout its range and make certain that voltage on associated test point can be varied from —10 V to +10 V.

o. Adjust each ADJUST control to obtain +1.5 Vdc at associated MEASURE test point.

p. Disconnect inputs from probe pod 3 and reconnect to probe pod 1.

q. Set up pulse generators to supply waveforms shown in figure 4-6.

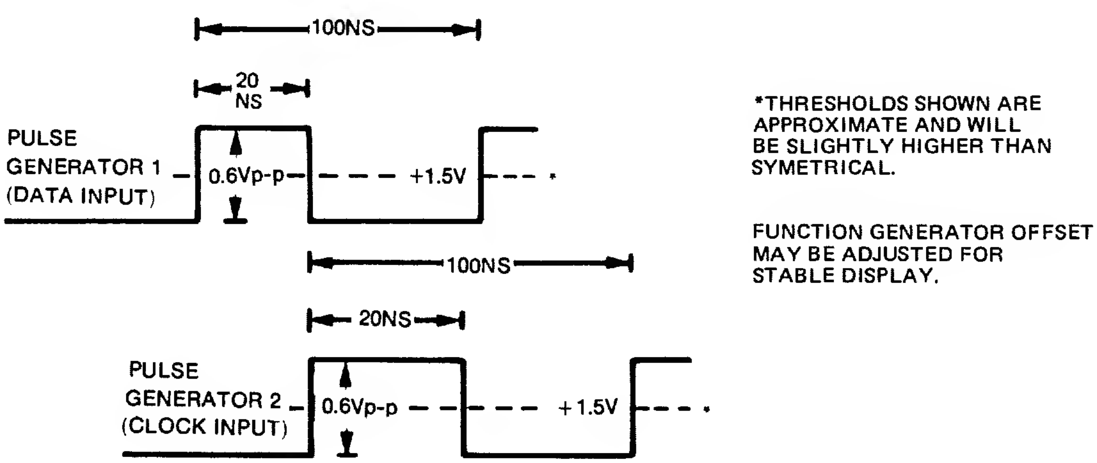


Figure 4-6. Minimum Input Voltage Swing Test Waveforms

r. Repeat steps c through 1, except leave PROBE THRESHOLD LEVEL switches in VARIABLE. This verifies 1615A minimum input swing specification of 0.6 V.

s. Connect multimeter to each probe input lead (+ side to probe channel, — side to probe ground). Multimeter should indicate 50 ± 5 kilohms.

t. Using LCR meter, measure shunt capacitance between each probe input lead and probe ground. Each input capacitance should be approximately 15 to 25 pF (probe capacitance without external wiring is ⩽14 pF.)

u. Reset PROBE THRESHOLD LEVEL switches to TTL.

PERFORMANCE TESTS

4-14. ASYNCHRONOUS OPERATION TEST.

SPECIFICATION:

MINIMUM DETECTABLE GLITCH: 5 ns with 30% peak overdrive or 250 mV, whichever is greater.
GLITCH TRIGGER: on any selected channel(s), if a glitch is captured, the glitch is AND'ed with the asynchronous pattern trigger.
PATTERN TRIGGER: any 8-bit pattern. Variable trigger duration 15, 50, 100, 200, 500, 1000 or 2000 ns ±15 ns or 15%, whichever is greater.
EXTERNAL TRIGGER PULSE WIDTH: 5 ns minimum with 30% peak overdrive or 250 mV, whichever is greater.

DESCRIPTION:

This procedure verifies the glitch detection, glitch triggering, external trigger, and asynchronous pattern triggering operation of the 1615A.

EQUIPMENT:

5-ns Pulse Generator.
Oscilloscope.
50-ohm Termination (see figure 4-1).

PROCEDURE:

a. Connect 1615A to test equipment according to figure 4-7. Use pulse generator with 5-ns pulse output capability.

b. Connect all probe pods to 1615A, but connect only data lead ∅ of pod 1 to pulse generator.

c. Adjust pulse generator to supply test waveform shown in figure 4-8.

d. Press FORMAT SPECIFICATION key.

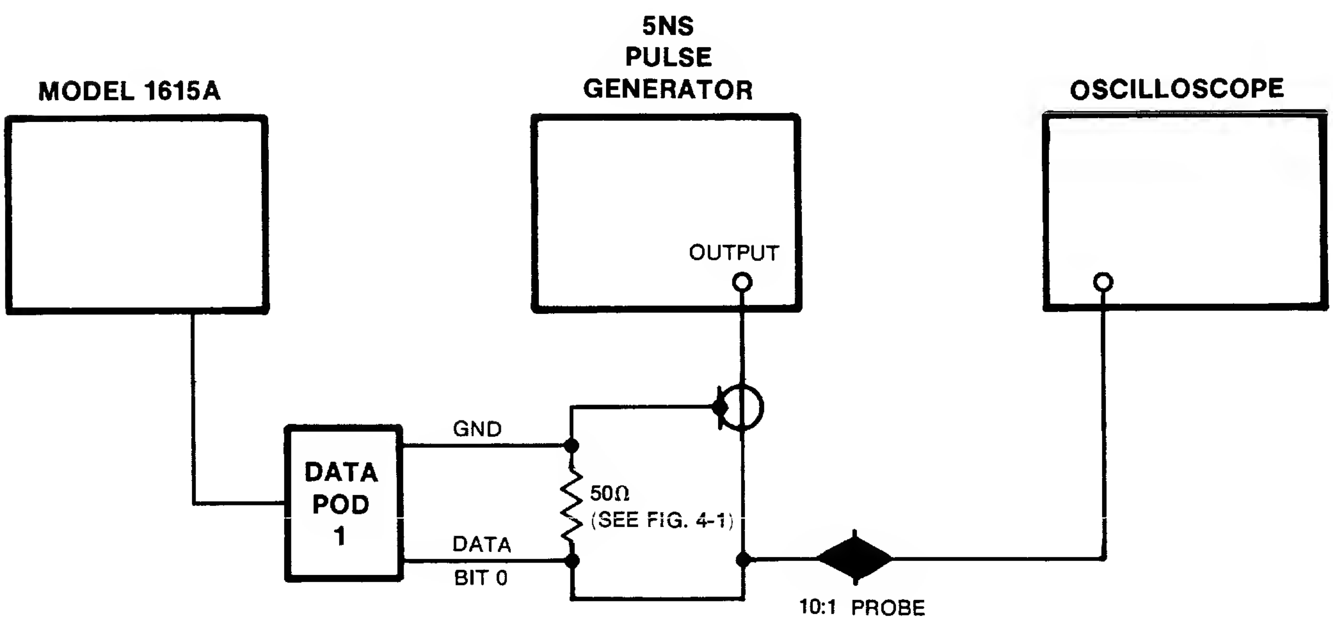


Figure 4-7. Asynchronous Specification Test Setup

PERFORMANCE TESTS

e. Use CURSOR keys to move cursor to each field in menu. Set up menu according to figure 4-9.

f. Press TRACE SPECIFICATION key.

g. Use CURSOR keys to move cursor to each field in menu. Set up menu according to figure 4-10.

h. Press TRACE key. Display will change to TRACE COMPLETE and show timing diagram with intensified vertical lines (glitches) on channel ∅ (GLITCH DISPLAY field must be ON). Move cursor to MAGNIFICATION field and press FIELD SELECT to expand display to clearly see glitches.

i. Disconnect bit ∅ and connect bit 1 to pulse generator output.

j. Press TRACE SPECIFICATION key.

k. Delete glitch requirement on channel ∅ and insert glitch requirement on channel 1.

l. Press TRACE key. Display will change to TRACE COMPLETE and show timing diagram with intensified vertical lines (glitches) on channel 1 display.

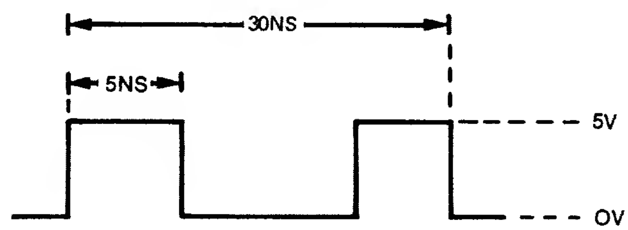


Figure 4-8. Asynchronous Operation Test Waveform

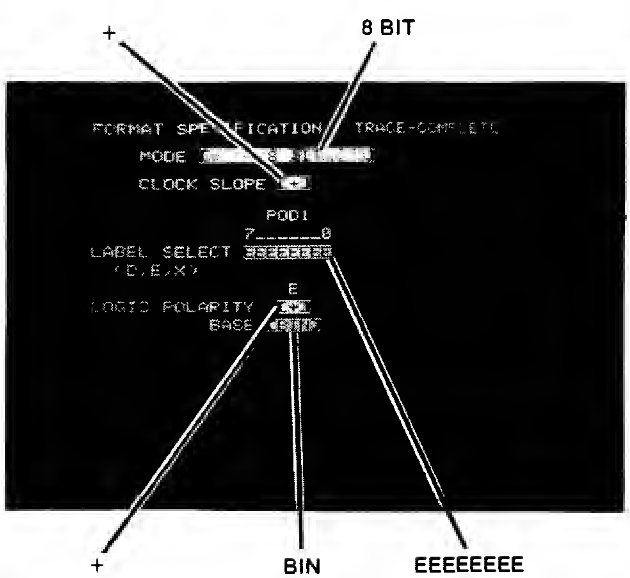


Figure 4-9. Asynchronous Tests Format Specification Menu

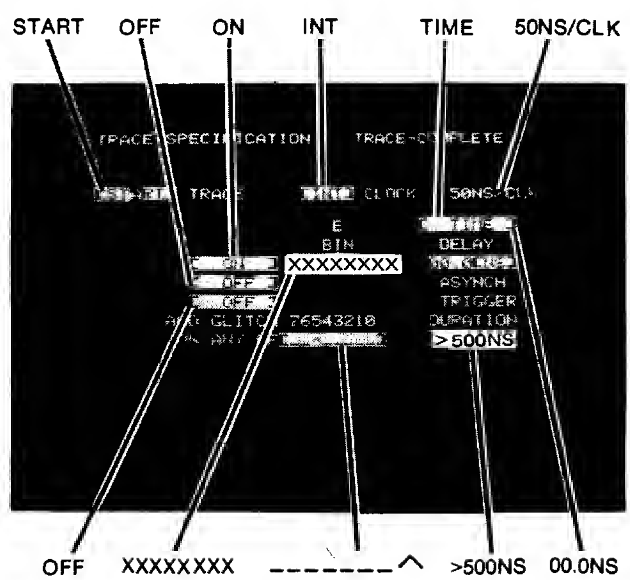


Figure 4-10. Asynchronous Tests Trace Specification Menu

m. Repeat steps i through l to check glitch triggering on channels 2 through 7. This verifies 1615A ability to detect and trigger on a minimum glitch in any selected channel.

n. Disconnect bit 7 and connect bit 1 to pulse generator output.

o. Press TRACE SPECIFICATION key.

p. Move cursor to glitch trigger field and delete glitch requirement (ANY GLITCH ON ANY OF - - - - - - - -).

q. Move cursor to trigger word field and select XXXXXX1X.

r. Set output of pulse generator for pulse width less than 500 ns.

s. Press TRACE key on 1615A. Display should show WARNING — NO 8 BIT TRIGGER.

t. Adjust pulse width from pulse generator for pulse greater than 500 ns. Display of 1615A should show TRACE COMPLETE. This verifies 1615A asynchronous pattern trigger with variable trigger duration.

u. Press TRACE SPECIFICATION key.

v. Move cursor to each field in menu. Set up menu according to figure 4-11.

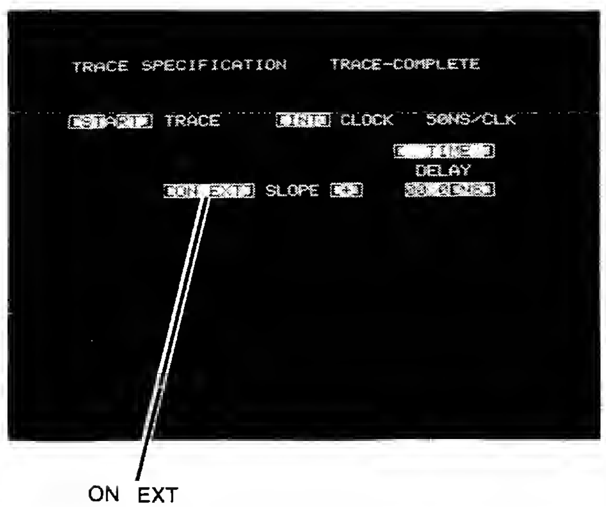


Figure 4-11. External Trigger Test Trace Specification Menu

w. Press TRACE key. Display will show TRACE — IN PROCESS and WARNING — NO 8 BIT TRIGGER.

x. Set pulse generator to supply 5-ns pulse width, 5-volt amplitude, 1-μsec repetition rate.

y. Connect clock probe EXT TRIG input to pulse generator output. Display of 1615A will show TRACE COMPLETE. This verifies 1615A acceptance of minimum external trigger on clock probe (at least 30% of the total pulse voltage or 250 mV, whichever is greater, must be above the threshold level for at least 5 ns).

PERFORMANCE TESTS

4-15. TRIGGER OUTPUTS (REAR PANEL) TEST.

SPECIFICATION:

LEVEL: high, ⩾+2 V into 50Ω.
low, ⩽+0.4 V into 50Ω.
DELAY FROM INPUT CLOCK: approx. 85 ns (16/24 BIT)
DELAY FROM PATTERN RECOGNITION TRIGGER AT PROBE: approx 45 ns plus asynchronous trigger duration width (8 BIT).

DESCRIPTION:

This test verifies the specified operation of the trigger and trace point outputs on the rear panel of the 1615A.

EQUIPMENT:

Oscilloscope
Pulse Generator
50-ohm Termination (see figure 4-1).

PROCEDURE:

a. Connect test equipment to 1615A as shown in figure 4-12.

b. Press FORMAT SPECIFICATION key on 1615A.

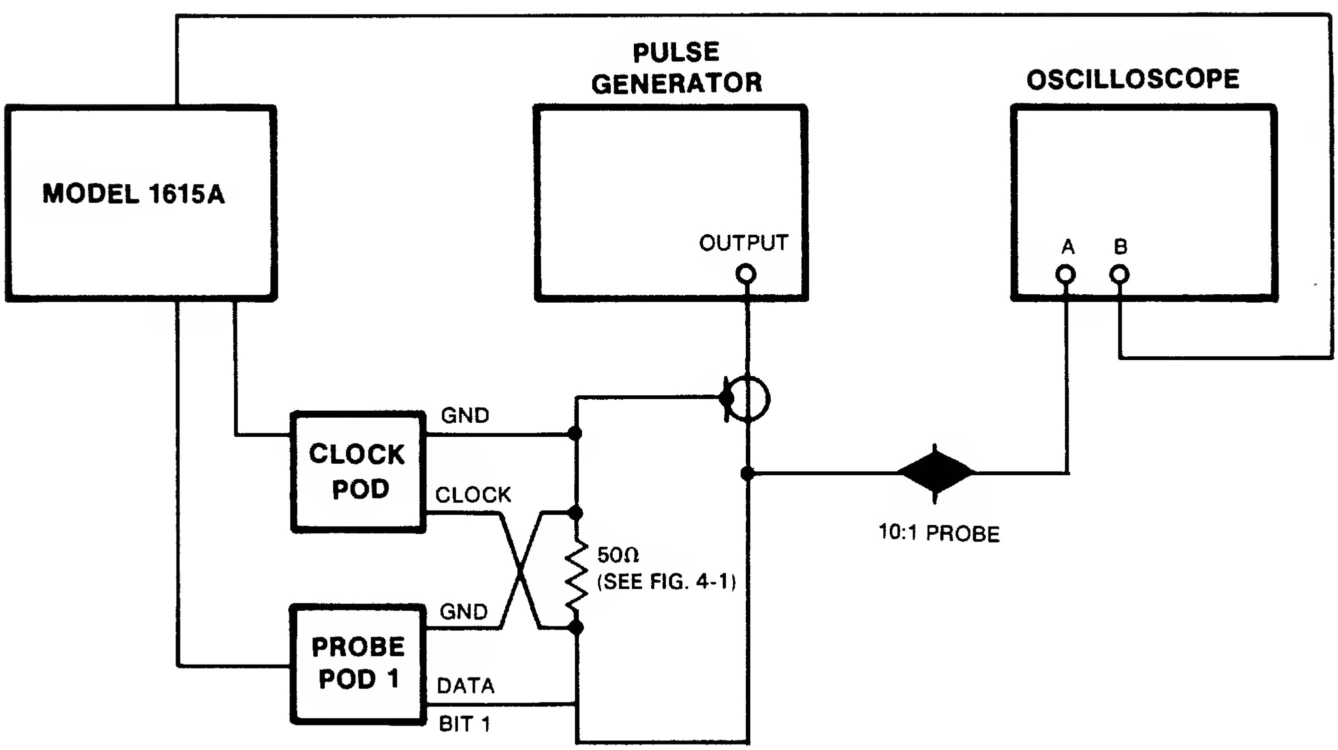


Figure 4-12 Trigger/Trace Point Outputs Test Setup

c. Use CURSOR keys to move cursor to each field in menu. Set up menu according to figure 4-13.

d. Press TRACE SPECIFICATION key.

e. Press DEFAULT key to format displayed menu in its most simple form.

f. Adjust pulse generator to supply waveform shown in figure 4-14 to 1615A.

g. Press TRACE key on 1615A. Hold key down to obtain TRACE CONTINUOUS indication on display.

h. Connect oscilloscope channel B to measure waveform at 16/24 BIT TRIG OUT on rear panel of 1615A. Oscilloscope should show high level of ⩽+0.4 V into 50Ω.

i. Disconnect oscilloscope channel B from 16/24 BIT TRACE OUT and connect to 16/24 BIT TRACE OUT on 1615A rear panel. Oscilloscope should show high level of ⩾+2 V into 50Ω and low level of ⩽+0.4 V into 50Ω. For more readable display, press TRACE SPECIFICATION key to increase repetition rate.

j. Press FORMAT SPECIFICATION key on 1615A.

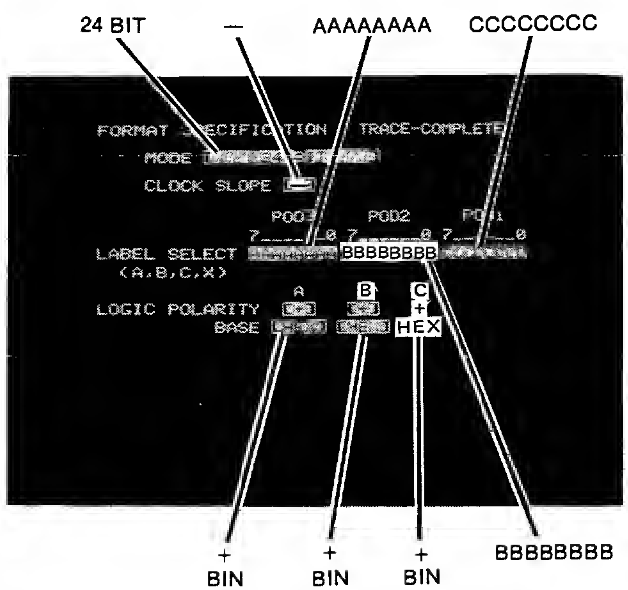


Figure 4-13. Trigger/Trace Point Outputs Format Specification

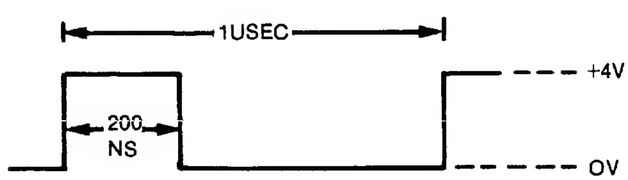


Figure 4-14. Trigger/Trace Point Outputs Test Waveform

PERFORMANCE TESTS

k. Press FIELD SELECT key to obtain 8 BIT MODE.

l. Press DEFAULT key to obtain most simple 8 BIT format specification menu.

m. Press TRACE SPECIFICATION key.

n. Press DEFAULT key to obtain most simple trace specification menu.

o. Move cursor into trigger ON field and enter XXXXXX1X.

p. Hold TRACE key down to obtain TRACE CONTINUOUS operation.

q. Connect oscilloscope channel B to monitor 8 BIT PATTERN OUT on rear panel of 1615A. Observe high level of $\geqslant$+2 V into 50Ω and low level, of $\leqslant$+0.4 V into 50Ω.

PERFORMANCE TEST RECORD

HEWLETT-PACKARD

MODEL 1615A

LOGIC ANALYZER

SERIAL NO. ____________

Tested by ____________

Date ____________

Paragraph Number	Test	Min	Results Actual	Max
4-13	Clock, Qualifier, and Data Inputs			
	Repetition Rate to 20 MHz	Valid Clock		
	Minimum Input Swing 0.6 V	Valid Clock and Data		
	Clock Pulse Width 20 ns	Valid Clock		
	Setup Time 20 ns	Valid Data		
	Hold Time 0	Valid Data		
	Input Threshold TTL +1.5 V Variable	±10 Vdc		
	Input RC	45 KΩ		55 KΩ ⩽14 pF
4-14	Asynchronous Operation			
	Minimum Detectable Glitch 5 ns	Glitch Indication		
	Glitch Trigger on any Selected Channel	Valid Trigger		
	Pattern Trigger, any 8-bit Pattern with Variable Duration.	Valid Trigger		
	External Trigger	Valid Trigger		
4-15	Trigger Outputs (Rear Panel)			
	16/24-bit Outputs Trigger High Level Trigger Low Level Trigger Delay approx 85 ns	 ⩾2 V		 ⩽0.4 V
	Trace High Level Trace Low Level Trace Delay approx 85 ns	⩾2 V		 ⩽0.4 V
	8-bit Output High Level Low Level Delay 45 ns + Async. Trig. Duration	 ⩾2 V		 ⩽0.4 V

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section contains a complete adjustment procedure for the 1615A. Perform the adjustment procedure only after instrument repairs. The adjustments can be made separately. These adjustments should not be part of a periodic maintenance program.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures.

5-3. EQUIPMENT REQUIRED.

5-4. A list of recommended test equipment is provided in Section I of this manual.

5-5. PREADJUSTMENT PROCEDURES.

a. Disconnect 1615A power cord.

b. Remove 1615A top cover.

c. Remove 1615A left side cover. (See figure 5-6.)

CAUTION

The adjustments are performed with the top and left side covers removed. Use care to avoid shorting or damaging internal parts of the instrument.

d. Reconnect 1615A power cord.

e. Press LINE switch to on position. The ON lamp should light.

ADJUSTMENTS

5-6. 5-VOLT POWER SUPPLY ADJUSTMENTS. (See figure 5-6 and schematic 2.)

a. Connect multimeter to test point +5 (A7TP2) and GND (A7TP4).

b. Adjust A7R12 for +5.13 volts on multimeter.

c. Connect multimeter to test point —5 (A7TP3) and GND (A7TP4).

d. Adjust A7R22 for —5.3 volts on multimeter.

ADJUSTMENTS

5-7. DISPLAY ALIGNMENT.

5-8. Normally it is not necessary to perform this procedure unless the CRT has been replaced.

a. Press LINE switch to off position and disconnect power cord.

b. Remove screw that secures post-accelerator lead to CRT shield.

c. Loosen four screws that hold CRT shield to main deck.

d. Remove CRT shield.

e. Loosen clamp on yoke L1.

f. Reconnect power cord and press LINE switch to on position.

g. Rotate yoke L1 so that horizontal lines on display are parallel with top and bottom of display window.

h. Press LINE switch to off position and disconnect power cord.

i. Tighten clamp on yoke L1.

CAUTION

Hand-tighten only. Excessive tightening will damage CRT.

j. Reinstall CRT shield and post-accelerator lead holder.

k. Reconnect power cord and press LINE switch to on position.

5-9. DISPLAY ADJUSTMENT. (See figure 5-7 and schematic 3.)

a. Press TIMING DIAG key.

b. Turn contrast adjustment A13R61 fully clockwise. This control is a service aid only. For normal operation, A13R61 should be fully clockwise.

c. Slowly adjust intensity control A13R60 clockwise until retrace lines can be seen. Then return A13R60 counterclockwise until desired brightness is obtained.

CAUTION

Excessive intensity will burn CRT phosphor, but this will not degrade display performance.

d. If vertical lines cannot be seen, adjust contrast control A6R21 (figure 5-6) for desired display contrast.

e. Adjust focus control A13R45 for best overall focus of display.

f. Set horizontal size A13R6 and vertical size A13R18 fully counterclockwise.

g. Adjust horizontal position A13R14 and vertical position A13R40 to center display.

h. Adjust linearity control A13R23 so that characters in top and bottom lines of display are same height.

i. Adjust horizontal size A13R6 and horizontal position A13R14 for 20 mm (0.8 in.) margin on each side of display.

j. Adjust vertical size A13R18 and vertical position A13R40 for 5 mm (0.2 in.) margin at top and bottom.

k. Repeat step h.

ADJUSTMENTS

5-10. TIMING ADJUSTMENTS. (See figures 5-1 and 5-8, and schematic 7A.)

5-11. Timing adjustments should only be checked and adjusted after repair of assembly A2 or a data acquisition malfunction.

a. Set LINE power switch to off position.

b. Remove assembly A2.

c. Intall extender board.

d. Install A2 on extender board.

e. Connect oscilloscope input A to A2TP1 and input B to A2TP2, the 8-bit clock strobe timing test points.

f. Connect clock probe input to SELF-TEST CLOCK and connect clock probe ground to COMMON on 1615A front panel.

g. Set LINE power switch to on position.

h. Press TRACE key. Oscilloscope should show waveforms in figure 5-1.

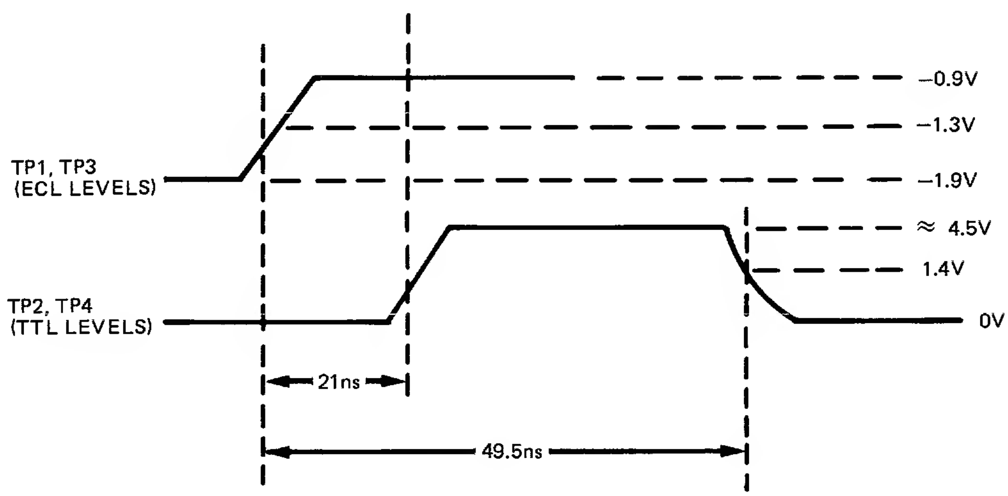


Figure 5-1. Timing Generator Clock Strobe Waveforms

i. Adjust A2R10 (E20) for 21 ns between leading edges of A2TP1 and A2TP2 waveforms.

j. Adjust A2R11 (E49) for 49.5 ns between leading edge of A2TP1 waveform and trailing edge of A2TP2 waveform.

k. Connect oscilloscope input A to A2TP3 and input B to A2TP4, the 16-bit clock strobe timing test points.

l. Adjust A2R12 (A20) for 21 ns between leading edges of A2TP3 and A2TP4 waveforms.

m. Adjust A2R11 (A49) for 49.5 ns between leading edge of A2TP3 waveform and trailing edge of A2TP4 waveform.

ADJUSTMENTS

5-12. FILTER WIDTH ADJUSTMENT. (See figures 5-2 through 5-6, and schematic 5A.)

a. Press FORMAT SPECIFICATION key.

b. Set up format specification according to figure 5-2.

c. Press TRACE SPECIFICATION key.

d. Set up trace specification according to figure 5-3.

e. Connect instruments according to test setup in figure 5-4.

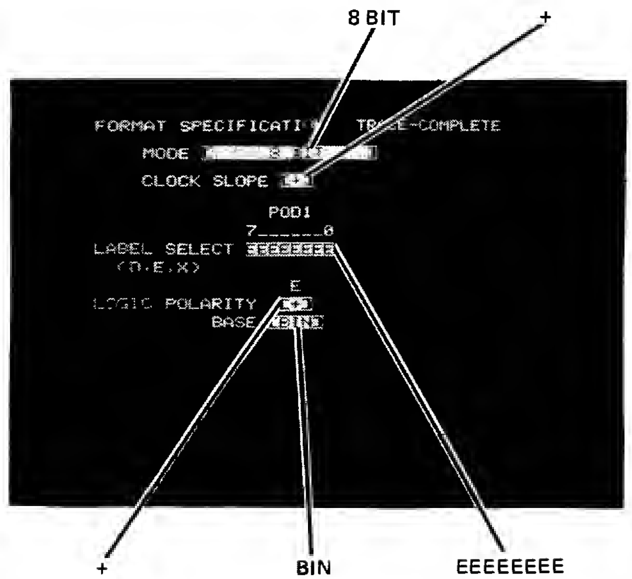


Figure 5-2. Format Specification for Filter Width Adjustment

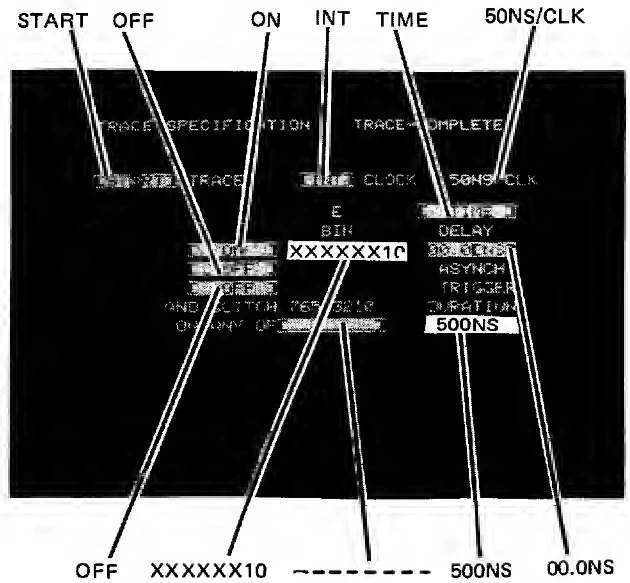


Figure 5-3. Trace Specification for Filter Width Adjustment

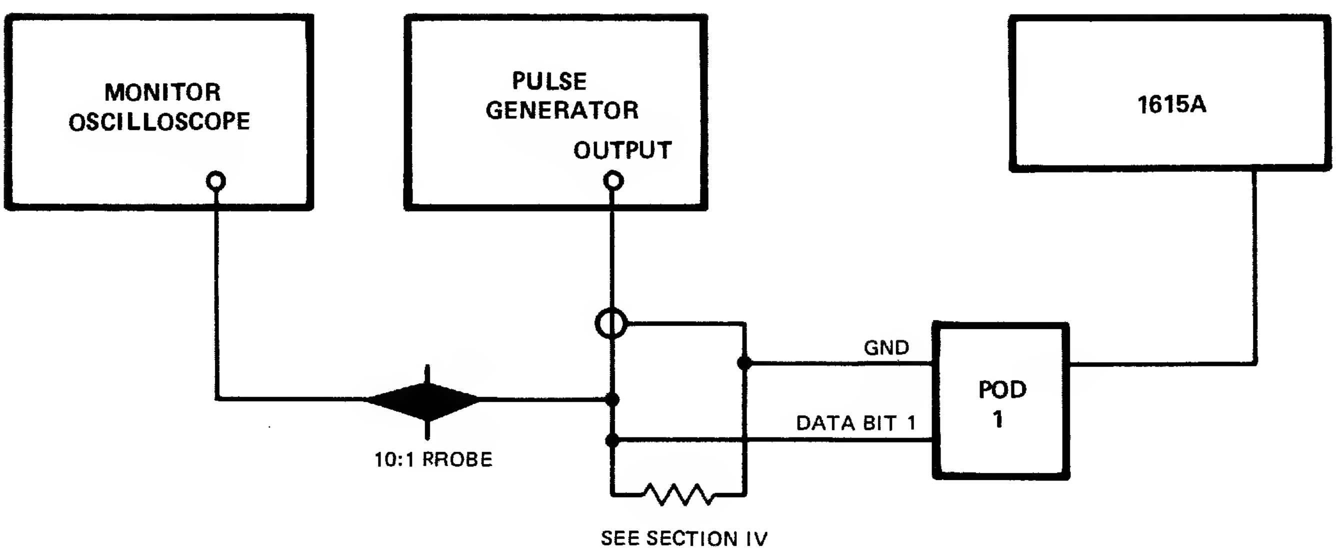


Figure 5-4. Filter Width Adjustment Test Setup

f. Adjust pulse generator to provide waveform with parameters as shown in figure 5-5.

g. Set filter adjustment A4R20 fully clockwise.

h. Press and release TRACE key.

i. Readjust A4R20 counterclockwise until 1615A just triggers on 500-ns pulse.

j. Repeat steps h and i to obtain the best adjustment of A4R20.

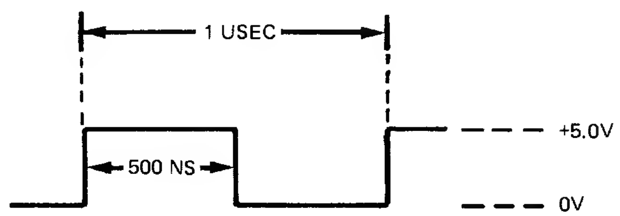


Figure 5-5. Filter Width Adjustment Waveform

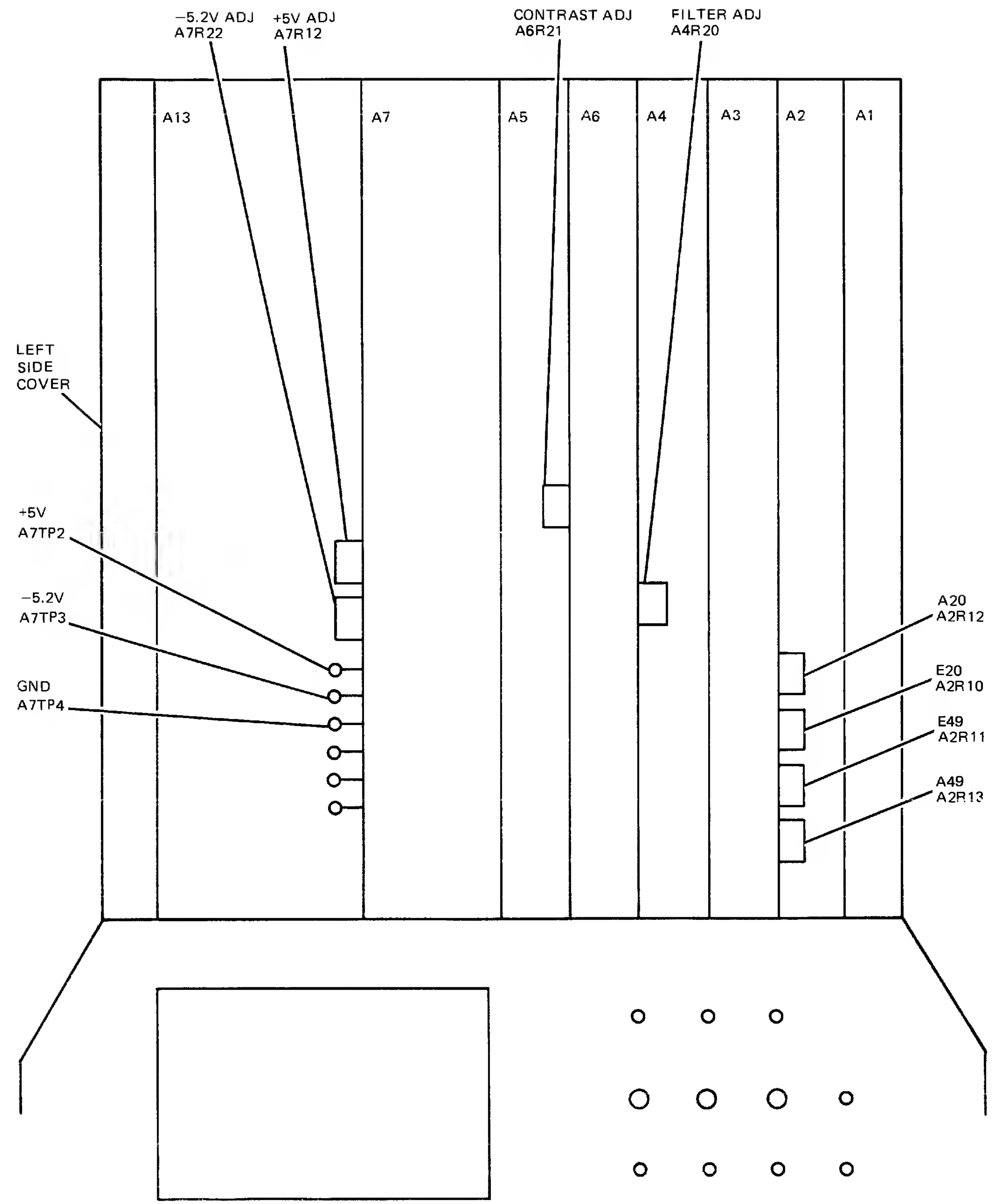
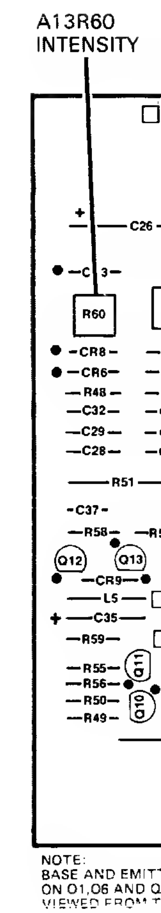
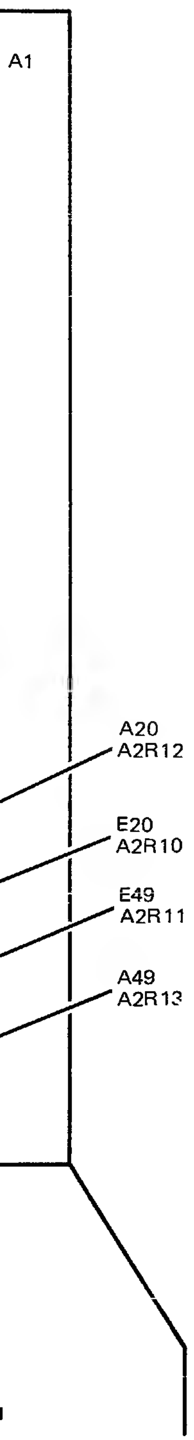


Figure 5-6. Adjustment Locations, Top View





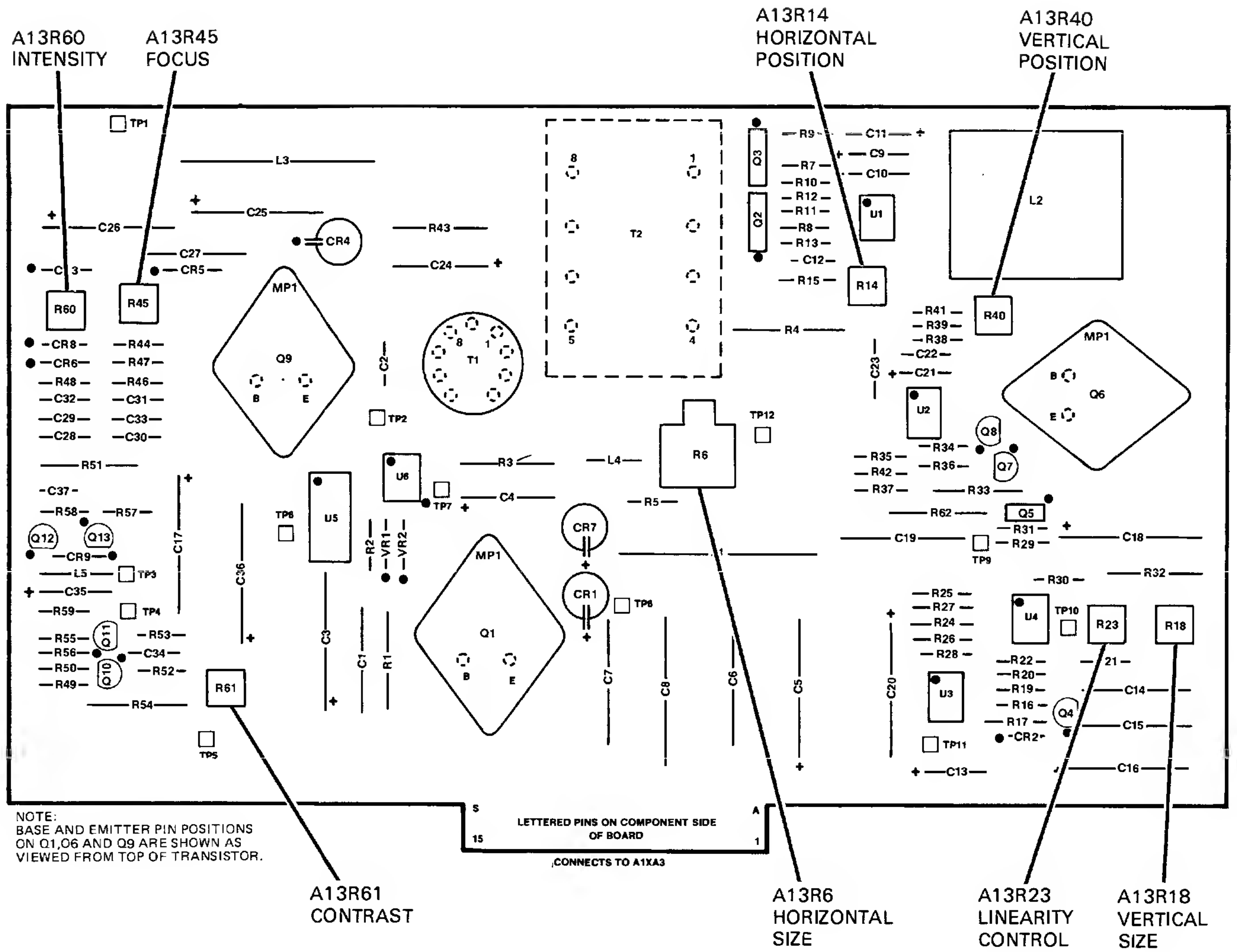


Figure 5-7. Adjustment Locations, Display Assembly A13

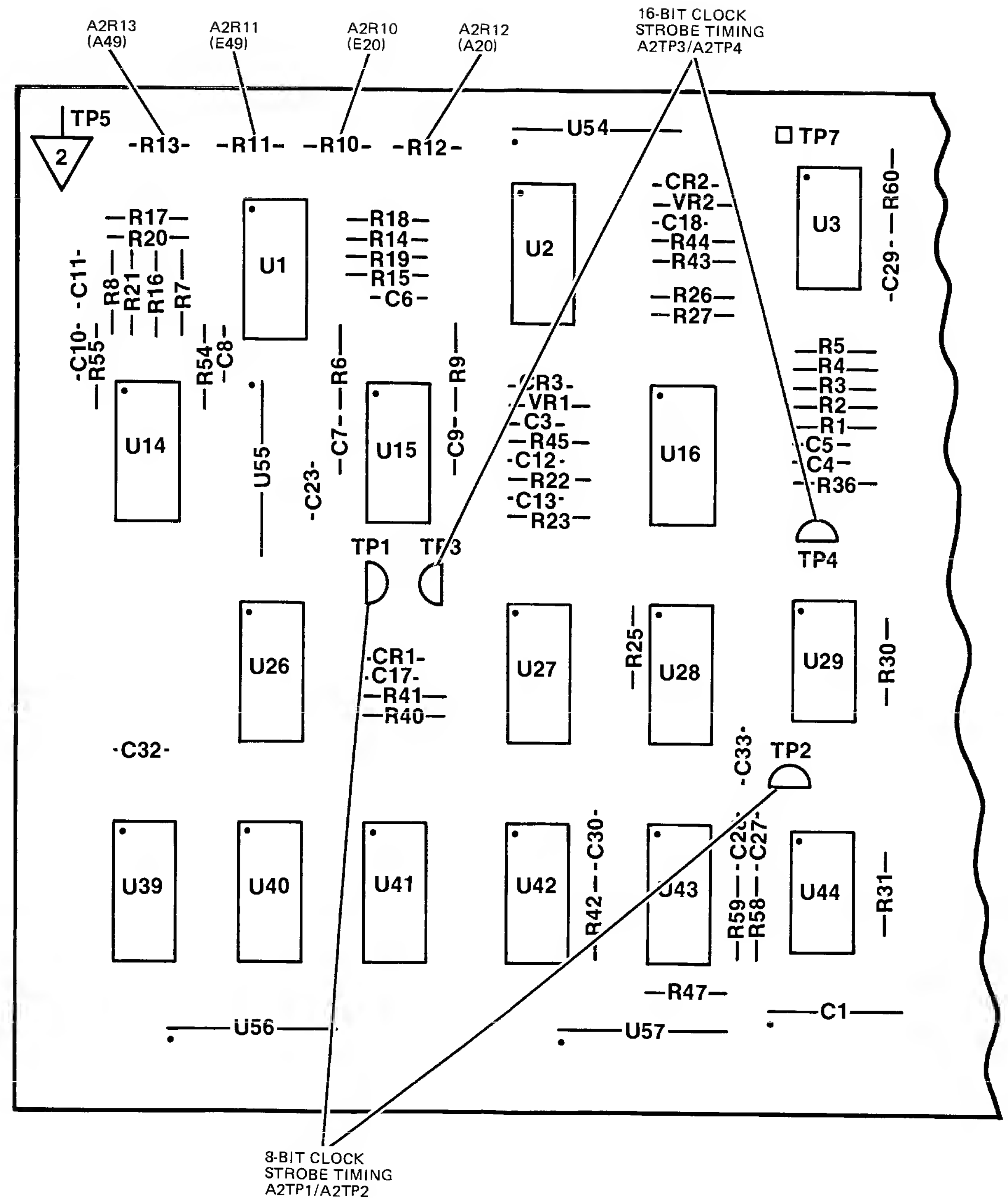
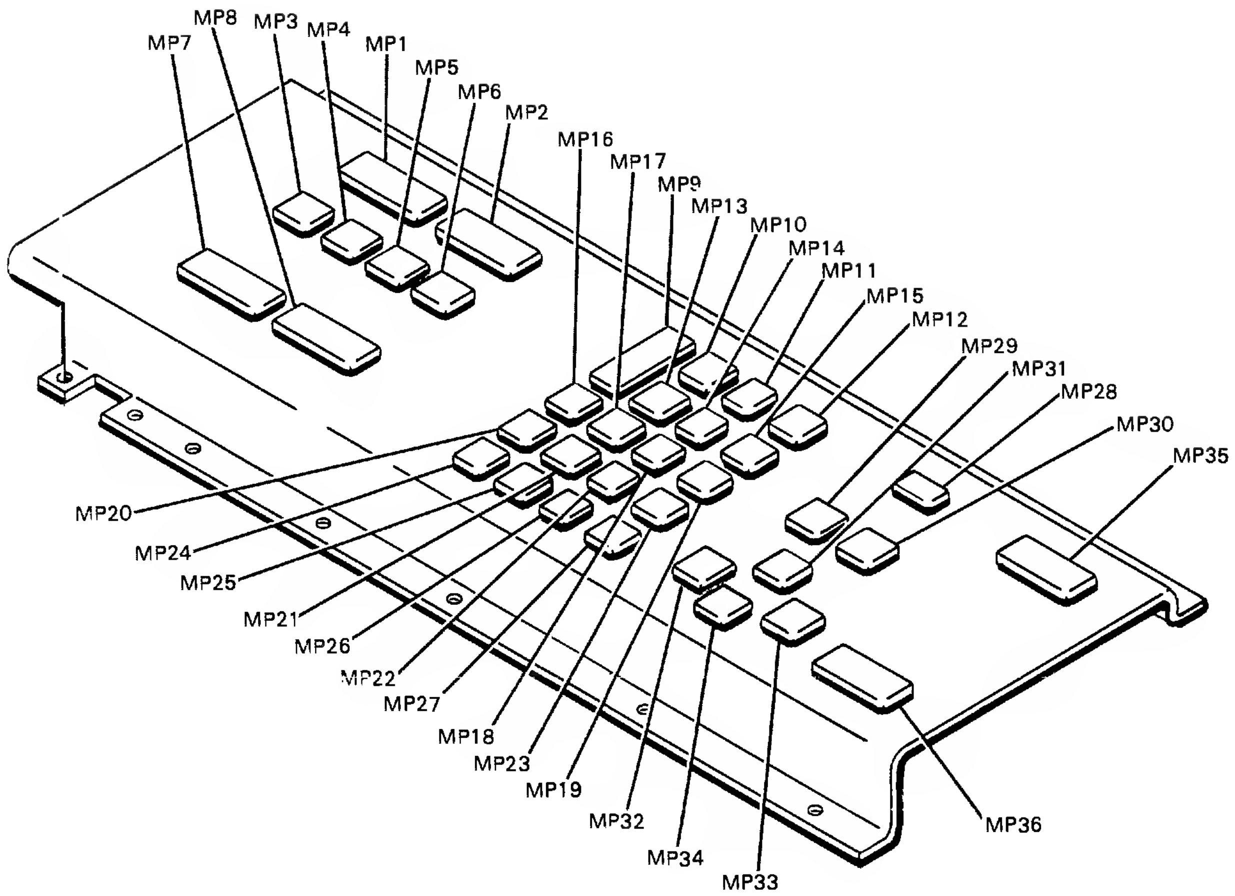


Figure 5-8. Timing Adjustment Locations, Assembly A2

DETAIL A



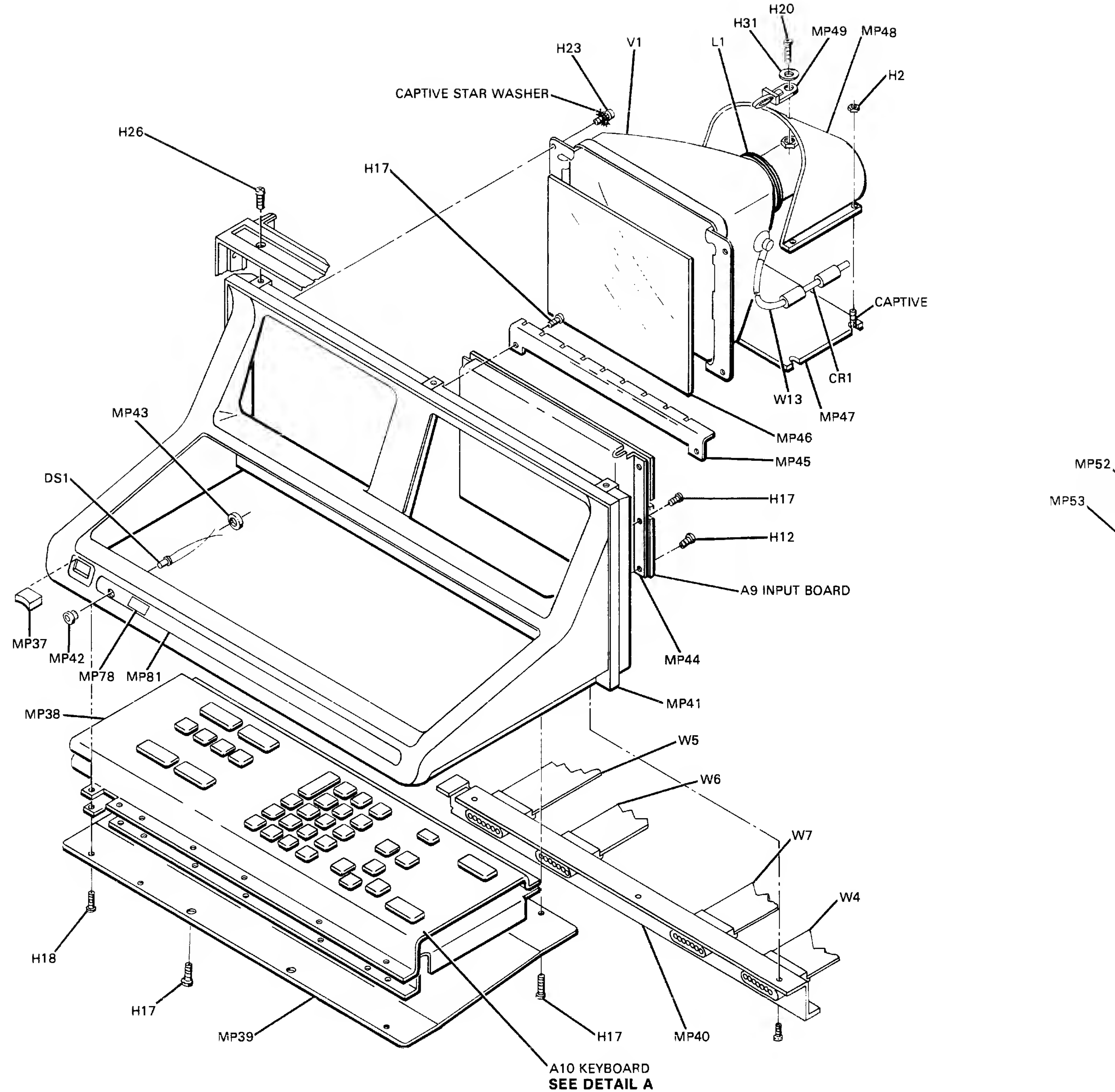


Figure 6-1. 1615A Front Portion Exploded View

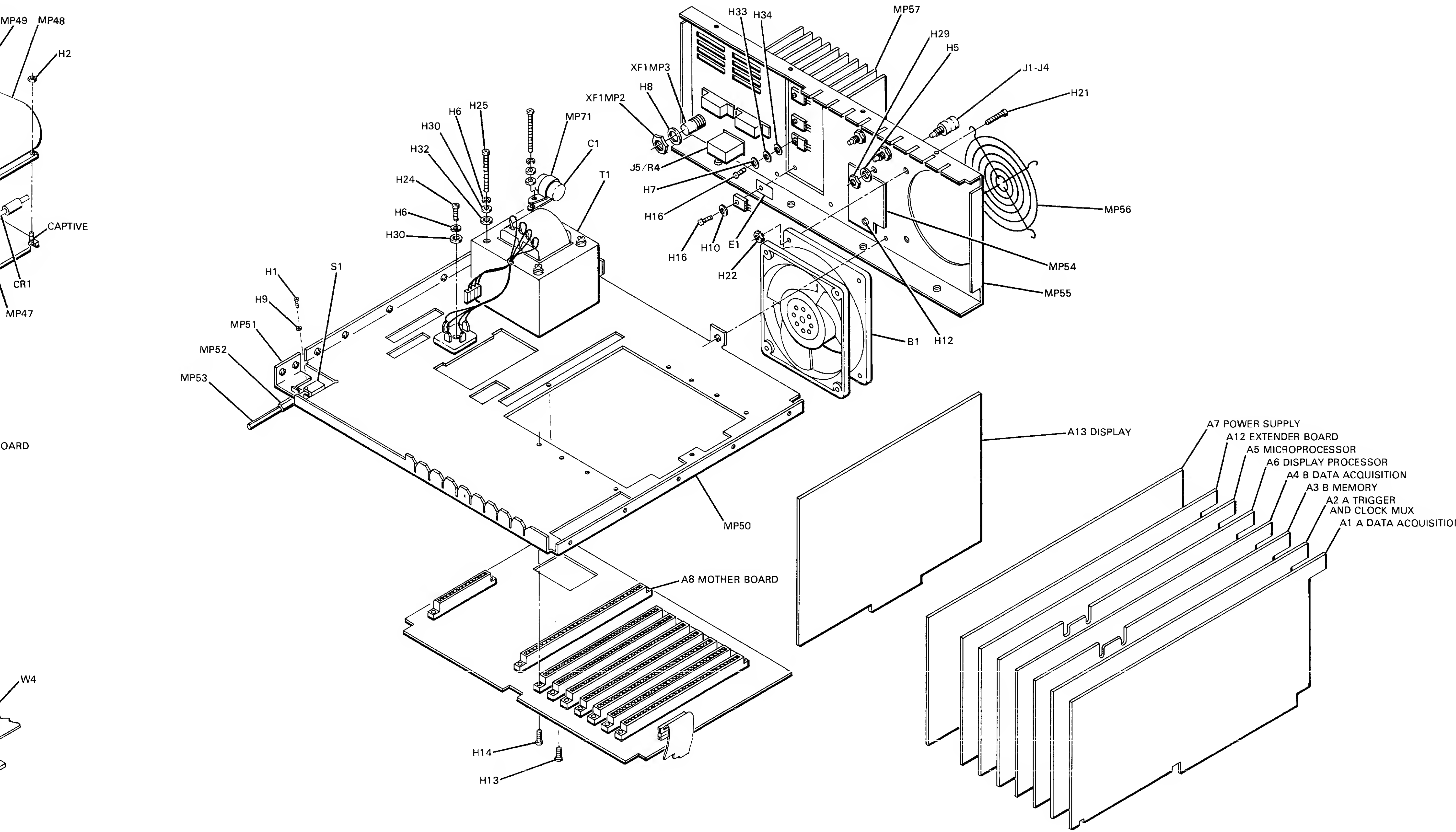


Figure 6-2. 1615A Rear Portion Exploded View

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains material lists for ordering replaceable parts. The material lists are divided into levels of assembly with the material list of parts used in the final assembly first followed by material lists for each of the subassemblies.

6-3. The information given for each part consists of the following:

a. Reference designation(s) assigned to the part(s).

b. Hewlett-Packard Part Number.

c. Total qualtity of the part(s) used in the assembly.

d. Description of the part.

6-4. ORDERING INFORMATION.

6-5. To order a part listed in the material lists, quote the Hewlett-Packard Part Number, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

6-6. To order a part that is not listed in the material lists, include the instrument model number, instrument serial number, a description of the part (including its function), and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-7. DIRECT MAIL ORDER SYSTEM.

6-8. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are:

Direct ordering and shipment from the HP Parts Center in Mountain View, California.

No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

Prepaid transportation (there is a small handling charge for each order).

No invoices — to provide these advantages, a check or money order must accompany each order.

6-9. Mail order forms and specific ordering information is available through your local HP office.

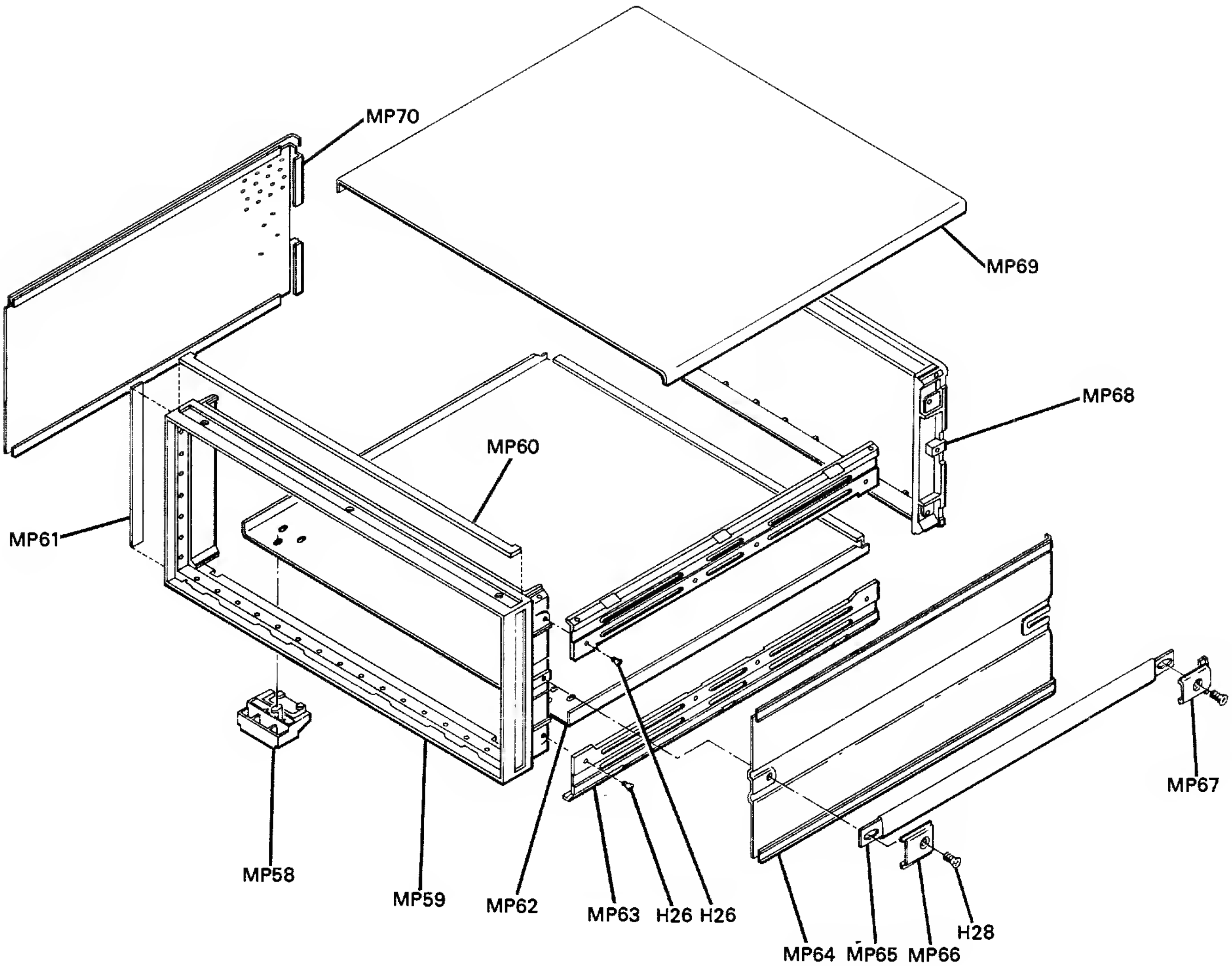


Figure 6-3. 1615A Frame Exploded View

Table 6-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
A1	01615-66501	5		BOARD ASSEMBLY, STATE DATA ACQ.	28480	01615-66501
A2	01615-66502	6		BOARD ASSEMBLY, TRIGGER AND CLOCK	28480	01615-66502
A3	01615-66503	7		BOARD ASSEMBLY, MEMORY	28480	01615-66503
A4	01615-66504	8		BOARD ASSEMBLY, TIMING DATA ACQ.	28480	01615-66504
A5	01615-66517	1		BOARD ASSEMBLY, MICROPROCESSOR AND ROM	28480	01615-66517
A6	01615-66516	2		BOARD ASSEMBLY, DISPLAY PROGRAMMER	28480	01615-66516
A7	01615-66513	9		BOARD ASSEMBLY, POWER SUPPLY	28480	01615-66513
A8	01615-66508	2		BOARD ASSEMBLY, MOTHER	28480	01615-66508
A9	01615-66509	3		BOARD ASSEMBLY, PROBE THRESHOLD/INPUT	28480	01615-66509
A10	01615-66510	6		BOARD ASSEMBLY, KEYBOARD	28480	01615-66510
A12	01615-66512	8		BOARD ASSEMBLY, EXTENDER	28480	01615-66512
A13	01611-66503	3		BOARD ASSEMBLY, DISPLAY DRIVER	28480	01611-66503
B1	3160-0262	9	1	FAN-TBAX 54-CFM 105-125V 50/60-HZ	0653A	760-125XL-2182-11115
C1	0160-4026	8	1	CAPACITOR-FXD .2UF +-20% 250VDC PPR	28480	0160-4026
CR1	1901-0768	0	1	DIODE-HV RECT 20KV 600UA 300NS	27777	H617
CR2	1906-0093	4	1	DIODE-FW BRDG 100V 35A	04713	MDA3501
DS1	1990-0524	3	1	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4550
E1	0340-0511	0	4	INSULATOR-XSTR KAPTON USED ON Q1 AND 2, U1 AND 2	28480	0340-0511
E2	01615-01204	9	1	STRAP-GROUNDING, BETWEEN MP40 AND MP41	28480	01615-01204
E3	0360-0001	5	1	CRT CLAMP GROUNDING	28480	0360-0001
F1	2110-0014	3	1	FUSE 4A 250V SLO-BLO 1.25X.25 UL	75915	313004
F1	2110-0303	3	1	FUSE 2A 250V SLO-BLO 1.25X.25 UL	28480	2110-0303
H1	0520-0127	6	2	SCREW-MACH 2-56 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H2	0590-0076	1	4	NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H3	1251-0218	6	8	LOCK-SUBMIN D CONN (ATTACH HARDWARE FOR J5 THRU J8)	28480	1251-0218
H4	2190-0011	8	4	WASHER-LK INTL T NO. 10 .195-IN-ID (FOR A8C1, A8C2)	28480	2190-0011
H5	2190-0016	3	4	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
H6	2190-0017	4	5	WASHER-LK HLCL NO. 8 .168-IN-ID	28480	2190-0017
H7	2190-0019	6		WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
H8	2190-0037	8	1	WASHER-LK INTL T 1/2 IN .512-IN-ID	28480	2190-0037
H9	2190-0045	8	2	WASHER-LK HLCL NO. 2 .088-IN-ID	28480	2190-0045
H10	2190-0910	6	2	WASHER-LK INTL T NO. 4 .12-IN-ID	28480	2190-0910
H11	2200-0101	0	5	SCREW-MACH 4-40 .188-IN-LG PAN-HD-POZI (FOR HP82)	00000	ORDER BY DESCRIPTION
H12	2200-0103	2	4	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H13	2200-0105	4	11	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H14	2200-0109	8	12	SCREW-MACH 4-40 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H15	2200-0141	8	2	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI (FOR J5)	00000	ORDER BY DESCRIPTION
H16	2200-0143	0	4	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H17	2360-0115	4		SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H18	2360-0117	6	2	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H20	2360-0197	2	1	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI (TOP OF CRT CURVED SHIELD)	00000	ORDER BY DESCRIPTION
H21	2360-0203	1	4	SCREW-MACH 6-32 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H22	2420-0001	5		NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
H23	2510-0043	6	13	SCREW-MACH 8-32 .312-IN-LG PAN-HD-POZI (HOLD MAIN DECK TO MP63)	00000	ORDER BY DESCRIPTION
H24	2510-0111	9	1	SCREW-MACH 8-32 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H25	2510-0137	9	4	SCREW-MACH 8-32 2.75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H26	2510-0192	6	16	SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
H27	2680-0099	1	4	SCREW-MACH 10-32 .375-IN-LG PAN-HD-POZI (FOR A8C1, A8C2)	00000	ORDER BY DESCRIPTION
H28	2680-0172	1	2	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H29	2950-0001	8	4	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H30	3050-0001	1	9	WASHER-FL MTLC NO. 8 .172-IN-ID	28480	3050-0001
H31	3050-0010	2	1	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0010
H32	3050-0152	3	3	WASHER-SHLDR NO. 8 .172-IN-ID .438-IN-OD	28480	3050-0152
H33	3050-0235	3		WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
H34	3050-0791	6	2	INSULATOR-XSTR NYLON	28480	3050-0791
H35	3050-0931	6	2	WASHER-FL NM 1 1/8 IN 1.125-IN-ID (FOR A8C1, A8C2)	28480	3050-0931
J1	1250-0083	1	4	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J2	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J3	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J4	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J5	1251-4470	0	1	CONNECTOR-AC PWR CEE-22 MALE REC-FLG	28480	1251-4470

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
L1	01611-61603	4	1	YOKE ASSEMBLY, CRT	28480	01611-61603
MP1	5041-0735	1	1	KEYCAP FORMAT SPECIFICATION	28480	5041-0735
MP2	5041-0665	6	1	KEYCAP TRACE SPECIFICATION	28480	5041-0665
MP3	5041-0661	2	1	KEYCAP LIST	28480	5041-0661
MP4	5041-0955	7	1	KEYCAP TIMING DIAG	28480	5041-0955
MP5	5041-0954	6	1	KEYCAP CHAN SEQ	28480	5041-0954
MP6	5041-0763	5	1	KEYCAP AT TRIG WORD	28480	5041-0763
MP7	5041-0667	8	2	KEYCAP ROLL DISPLAY ARROW	28480	5041-0667
MP8	5041-0667	8		KEYCAP ROLL DISPLAY ARROW	28480	5041-0667
MP9	5041-0666	7	1	KEYCAP FIELD SELECT	28480	5041-0666
MP10	5041-0043	4	1	KEYCAP D	28480	5041-0043
MP11	5041-0044	5	1	KEYCAP E	28480	5041-0044
MP12	5041-0045	6	1	KEYCAP F	28480	5041-0045
MP13	5041-0040	1	1	KEYCAP A	28480	5041-0040
MP14	5041-0041	2	1	KEYCAP B	28480	5041-0041
MP15	5041-0042	3	1	KEYCAP C	28480	5041-0042
MP16	5041-0956	8	1	KEYCAP X DON'T CARE	28480	5041-0956
MP17	5041-0682	7	1	KEYCAP 7	28480	5041-0682
MP18	5041-0683	8	1	KEYCAP 8	28480	5041-0683
MP19	5041-0684	9	1	KEYCAP 9	28480	5041-0684
MP20	5041-0820	5	1	KEYCAP DECIMAL POINT	28480	5041-0820
MP21	5041-0679	2	1	KEYCAP 4	28480	5041-0679
MP22	5041-0680	5	1	KEYCAP 5	28480	5041-0680
MP23	5041-0681	6	1	KEYCAP 6	28480	5041-0681
MP24	5041-0685	0	1	KEYCAP 7	28480	5041-0685
MP25	5041-0676	9	1	KEYCAP 1	28480	5041-0676
MP26	5041-0677	0	1	KEYCAP 2	28480	5041-0677
MP27	5041-0678	1	1	KEYCAP 3	28480	5041-0678
MP28	5041-0301	7	1	KEYCAP BLANK	28480	5041-0301
MP29	5041-0660	1	1	KEYCAP DECR	28480	5041-0660
MP30	5041-0659	8	1	KEYCAP INCR	28480	5041-0659
MP31	5041-0686	1	4	KEYCAP CURSOR ARROW	28480	5041-0686
MP32	5041-0686	1		KEYCAP CURSOR ARROW	28480	5041-0686
MP33	5041-0686	1		KEYCAP CURSOR ARROW	28480	5041-0686
MP34	5041-0686	1		KEYCAP CURSOR ARROW	28480	5041-0686
MP35	5041-0631	6	1	KEYCAP TRACE	28480	5041-0631
MP36	5041-0664	5	1	KEYCAP STOP	28480	5041-0664
MP37	0370-2989	3	1	KEYCAP LINE POWER SWITCH	28480	0370-2989
MP38	01615-00201	4	1	PANEL, KEYBOARD	28480	01615-00201
MP39	01615-04101	1	1	COVER, KEYBOARD, BOTTOM	28480	01615-04101
MP40	01615-01201	6	1	BRACKET, PROBE CONNECT	28480	01615-01201
MP41	5040-0564	2	1	SUPPORT KEYBOARD	28480	5040-0564
MP42	1400-0547	1	1	CL-LED-MTG	28480	1400-0547
MP43	1400-0540	4	1	RETAINER RING-LED CLIP 0.270-IN SEPRATED	28480	1400-0540
MP44	01615-00203	6	1	PANEL, INPUT	28480	01615-00203
MP45	01615-01202	7	1	BRACKET, PC BOARD FRONT	28480	01615-01202
MP46	01611-24101	9	1	SAFETY SHIELD, CRT	28480	01611-24101
MP47	01611-00602	5	1	SHIELD, CRT, FLAT	28480	01611-00602
MP48	01611-00601	4	1	SHIELD, CRT CURVED	28480	01611-00601
MP49	1400-0335	5	1	CABLE TIE 1.75-DIA .188-WD NYL	28480	1400-0335
MP50	01615-00101	3	1	MAIN DECK	28480	01615-00101
MP51	01615-01203	8	1	BRACKET, LINE SWITCH MOUNTING	28480	01615-01203
MP52	01830-23201	3	1	COUPLER, LINE POWER SWITCH	28480	01830-23201
MP53	01611-23701	3	1	SHAFT, LINE POWER SWITCH	28480	01611-23701
MP54	01615-04103	3	1	COVER, HP-IB CONNECTOR	28480	01615-04103
MP55	01615-00204	7	1	PANEL, REAR	28480	01615-00204
MP56	3160-0092	3	1	FINGER GUARD	28480	3160-0092
MP57	01615-21101	7	1	HEAT SINK	28480	01615-21101
MP58	5040-7201	8	4	FOOT(STANDARD)	28480	5040-7201
MP59	5020-8805	8	1	FRAME FRONT	28480	5020-8805
MP60	5040-7202	9	1	TRIM, TOP	28480	5040-7202
MP61	5001-0440	1	2	TRIM, SIDE	28480	5001-0440
MP62	5060-9846	3	1	COVER BOTTOM	28480	5060-9846
MP63	5020-8836	5	4	STRUT CORNER	28480	5020-8836
MP64	5060-9883	8	1	COVER SIDE WITH HANDLE	28480	5060-9883
MP65	5060-9803	2	1	STRAP HANDLE ASSEMBLY	28480	5060-9803
MP66	5040-7219	8	1	FRONT	28480	5040-7219
MP67	5040-7220	1	1	REAR	28480	5040-7220
MP68	5020-8806	9	1	FRAME REAR	28480	5020-8806
MP69	5061-1953	9	1	COVER TOP	28480	5061-1953
MP70	5060-9916	8	1	COVER SIDE PERFORATED	28480	5060-9916
MP71	1400-0016	9	1	CLAMP-CABLE .75-DIA .5-WD NYL	28480	1400-0016
MP72	0340-0553	0	3	INSULATOR-FLG-BSHG NYLON BLACK (FOR ADJUST POTS ON A9)	28480	0340-0553
MP73	1400-0090	9	1	FUSEHOLDER COMPONENT FOR USE ON (FOR XF1)	28480	1400-0090

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP74	1400-0916	8	2	CLAMP-CABLE .255-DIA .5-WD ABS (FOR FAN POWER CABLE)	95987	HPC-25
MP75	1540-0325	9	1	CASE-CRYGPVC 16LG 9.25WD 3DP (FOR ACCESSORIES)	28480	1540-0325
MP76	5040-0588	0	1	EXTERNAL, SLIP-ON	28480	5040-0588
MP77	5951-1125	4	1	LABEL;SERIAL NO.	28480	5951-1125
MP78	7120-1254	1	1	NAMEPLATE .312-IN-WD .54-IN-LG AL	28480	7120-1254
MP79	7120-4184	2	1	LABEL-IDENTIFICATION 1-IN-WD 2.5-IN-LG	28480	7120-4184
MP80	7120-6264	3	2	LABEL (ON TRANSFORMER ON A13)	28480	7120-6264
MP81	7120-6491	8	1	LABEL, BELOW KEYBOARD	28480	7120-6491
MP82	01615-04102	2	1	COVER, PROBE CABLE BEHIND MP40,INSIDE 62	28480	01615-04102
Q1	1854-0768	9	2	TRANSISTOR NPN SI PD=90W FT=3MHZ	04713	MJE1661
Q2	1854-0768	9		TRANSISTOR NPN SI PD=90W FT=3MHZ	04713	MJE1661
R1	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R4	0687-4751	2	1	RESISTOR 4.7M 10% .5W CC TC=0+1000	01121	EB4751
S1	3101-1720	2	1	SWITCH-PB DPDT 4A 250VAC	28480	3101-1720
T1	9100-4034	1	1	TRANSFORMER-POWER PRI: 100/120/220/240	28480	9100-4034
U1	1826-0221	0	1	IC V RGLTR TO-220	04713	MC7912CT
U2	1826-0147	9	1	IC 7812 V RGLTR TO-220	04713	MC7812CP
V1	5061-1250	9	1	CRT	28480	5061-1250
W1	8120-1521	6	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT (SEE SECTION 2 FOR OTHER POWER CORDS)	28480	8120-1521
W2	01611-61602	3	1	CABLE, CRT	28480	01611-61602
W3	01615-61610	7	2	CABLE ASSEMBLY, 5VPS A7 TO Q2	28480	01615-61610
W4	01615-61601	6	1	CABLE, CLOCK PROBE	28480	01615-61601
W5	01615-61619	6	1	CABLE ASSEMBLY, PROBE POD 3	28480	01615-61619
W6	01615-61618	7	1	CABLE ASSEMBLY, PROBE POD 2	28480	01615-61618
W7	01615-61617	4	1	CABLE ASSEMBLY, PROBE POD 1	28480	01615-61617
W8	01600-61616	6	1	CABLE ASSEMBLY, A7 TO U1	28480	01600-61616
W9	01607-61613	0	1	CABLE ASSEMBLY, A7 TO U2	28480	01607-61613
W10	01615-61610	7		CABLE ASSEMBLY, 5VPS A7 TO Q1	28480	01615-61610
W11	01615-61609	4	1	CABLE ASSEMBLY,BRIDGE T1 TO CR2 AND A8	28480	01615-61609
W12	01615-61613	0	1	CABLE ASSEMBLY, LINW POWER SWITCH	28480	01615-61613
W13	8120-2309	0	1		28480	8120-2309
W14	01615-61608	3	1	CABLE, INTERCONNECT A3 TO A5	28480	01615-61608
W15	01615-61611	8	2	CABLE ASSEMBLY, GROUND STRAP, LONG	28480	01615-61611
W16	01615-61611	8		CABLE ASSEMBLY, GROUND STRAP, LONG	28480	01615-61611
W17	01615-61612	9	1	CABLE ASSEMBLY, GROUND STRAP, SHORT	28480	01615-61612
XF1MP1	2110-0465	8	1	FUSEHOLDER CAP EXTR PST; BAYONET; 20A	28480	2110-0465
XF1MP2	2110-0467	0	1	NUT-HEX 1/2-28 THD 0.688 A/F	75915	903-070
XF1MP3	2110-0470	5	1	FUSEHOLDER BODY EXTR PST; BAYONET; THD	75915	345003-010

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01615-66501	5	1	BOARD ASSEMBLY, STATE DATA ACQ.	28480	01615-66501
A1C1	0160-2055	9	112	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C5	0160-3443	1	14	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C8	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C9	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C12	0180-0229	7	12	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X901082
A1C13	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X901082
A1C14	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C34	0160-3466	8	1	CAPACITOR-FXD 100PF +-10% 1KVDC CER	28480	0160-3466
A1C35	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C36	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C37	0160-3470	4	4	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A1C38	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A1C39	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A1C40	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A1CR1	1901-0535	9	6	DIODE-SCHOTTKY	28480	1901-0535
A1CR2	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A1CR3	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A1P1	1251-4542	7	3	CONNECTOR 26-PIN M POST TYPE	28480	1251-4542
A1P2	1251-4542	7		CONNECTOR 26-PIN M POST TYPE	28480	1251-4542
A1P3	1251-4542	7		CONNECTOR 26-PIN M POST TYPE	28480	1251-4542
A1Q1	1853-0036	2	5	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A1Q2	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A1R1	0757-0284	7	30	RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A1R2	0757-0282	5	13	RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A1R5	0698-3446	3	2	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A1R7	0757-0280	3	78	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R8	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R9	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A1R10	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A1R11	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A1R12	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A1R13	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A1R14	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A1R15	0757-0428	1	2	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A1R16	0757-0428	1		RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A1R17	0757-0418	9	6	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A1R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R20	0757-0433	8	1	RESISTOR 3.32K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3321-F
A1R21	0757-0442	9	13	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R22	0757-0902	6	4	RESISTOR 120 2% .125W F TC=0+-100	24546	C4-1/8-T0-121-G
A1R23	0698-4157	5	12	RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R25	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R26	0757-0441	8	4	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A1R27	0698-5573	1	4	RESISTOR 50K .5% .125W F TC=0+-100	24546	C4-1/8-T0-5002-D
A1R28	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R29	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R30	0757-0902	6		RESISTOR 120 2% .125W F TC=0+-100	24546	C4-1/8-T0-121-G
A1R31	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R32	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R33	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R34	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A1R35	0698-5573	1		RESISTOR 50K .5% .125W F TC=0+-100	24546	C4-1/8-T0-5002-D
A1R36	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R37	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R38	0757-0902	6		RESISTOR 120 2% .125W F TC=0+-100	24546	C4-1/8-T0-121-G
A1R39	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R40	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R41	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R42	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A1R43	0698-5573	1		RESISTOR 50K .5% .125W F TC=0+-100	24546	C4-1/8-T0-5002-D
A1R44	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R45	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R46	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R47	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R48	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A1R49	0698-5573	1		RESISTOR 50K .5% .125W F TC=0+-100	24546	C4-1/8-T0-5002-D
A1R50	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R51	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R52	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
A1R53	0757-0902	6		RESISTOR 120 2% .125W F TC=0+-100	24546	C4-1/8-T0-121-G
A1R54	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R55	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A1R56	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A1R57	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A1TP1	0360-0535	0	39	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1U1	1816-1092	4	32	IC MEMORY	28480	1816-1092
A1U2	1816-1092	4		IC MEMORY	28480	1816-1092
A1U3	1816-1092	4		IC MEMORY	28480	1816-1092
A1U4	1816-1092	4		IC MEMORY	28480	1816-1092
A1U5	1816-1092	4		IC MEMORY	28480	1816-1092
A1U6	1816-1092	4		IC MEMORY	28480	1816-1092
A1U7	1816-1092	4		IC MEMORY	28480	1816-1092
A1U8	1816-1092	4		IC MEMORY	28480	1816-1092
A1U9	1816-1092	4		IC MEMORY	28480	1816-1092
A1U10	1816-1092	4		IC MEMORY	28480	1816-1092
A1U11	1816-1092	4		IC MEMORY	28480	1816-1092
A1U12	1816-1092	4		IC MEMORY	28480	1816-1092
A1U13	1816-1092	4		IC MEMORY	28480	1816-1092
A1U14	1816-1092	4		IC MEMORY	28480	1816-1092
A1U15	1816-1092	4		IC MEMORY	28480	1816-1092
A1U16	1816-1092	4		IC MEMORY	28480	1816-1092
A1U17	1816-1335	8	4	IC TTL S 256-BIT RAM 11-NS	04713	MCM10152L
A1U18	1820-2010	7	11	IC	28480	1820-2010
A1U19	1820-2010	7		IC	28480	1820-2010
A1U20	1816-1335	8		IC TTL S 256-BIT RAM 11-NS	04713	MCM10152L
A1U21	1820-2010	7		IC	28480	1820-2010
A1U22	1820-2010	7		IC	28480	1820-2010
A1U23	1820-1238	9	8	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A1U24	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A1U25	1820-1475	6	10	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U26	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U27	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A1U28	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A1U29	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U30	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U31	1820-1788	4	6	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U32	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U33	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U34	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U35	1820-1399	3	5	IC FF ECL D-TYPE COM CLOCK HEX	04713	MC10176P
A1U36	1820-1400	7	7	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A1U37	1820-0802	1	8	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U38	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A1U39	1820-0802	1		IC GATE ECL NOR QUAD 2-INR	04713	MC10102P
A1U40	1820-1400	7		IC GATE ECL AND QUAD 2-INR	04713	MC10104P
A1U41	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U42	1820-2010	7		IC	28480	1820-2010
A1U43	1820-1425	6	9	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INR	01295	SN74LS132N
A1U44	1820-0681	4	6	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U45	1820-1372	2	3	IC FF TTL S J-K BAR CLEAR DUAL	07263	74S109DC

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U46	1820-0809	8	7	IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A1U47	1820-0809	8		IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A1U48	1820-0809	8		IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A1U49	1820-0809	8		IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A1U50	1820-0809	8		IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A1U51	1820-0809	8		IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A1U52	1820-1399	3		IC FF ECL D-TYPE COM CLOCK HEX	04713	MC10176P
A1U53	1820-1399	3		IC FF ECL D-TYPE COM CLOCK HEX	04713	MC10176P
A1U54	1820-1399	3		IC FF ECL D-TYPE COM CLOCK HEX	04713	MC10176P
A1U55	1820-1399	3		IC FF ECL D-TYPE COM CLOCK HEX	04713	MC10176P
A1U56	1820-1173	1	6	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U57	1826-0524	6	2	IC OP AMP GP QUAD 14-DIP-P	27014	LM324AN
A1U58	1826-0524	6		IC OP AMP GP QUAD 14-DIP-P	27014	LM324AN
A1U59	1810-0273	9	26	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U60	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U61	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U62	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U63	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U64	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U65	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U66	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U67	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1XU17	1200-0607	0	19	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A1XU20	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A2	01615-66502	6	1	BOARD ASSEMBLY, TRIGGER AND CLOCK	28480	01615-66502
A2C1	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C4	0160-2200	6	4	CAPACITOR-FXD 43PF +-5% 300VDC MICA	28480	0160-2200
A2C5	0160-3446	4	1	CAPACITOR-FXD 220PF +-10% 1KVDC CER	28480	0160-3446
A2C6	0160-2200	6		CAPACITOR-FXD 43PF +-5% 300VDC MICA	28480	0160-2200
A2C7	0140-0192	9	3	CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A2C8	0140-0198	5	2	CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A2C9	0140-0192	9		CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A2C10	0140-0198	5		CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A2C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C14	0160-2200	6		CAPACITOR-FXD 43PF +-5% 300VDC MICA	28480	0160-2200
A2C15	0160-2198	1	9	CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A2C16	0140-0192	9		CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A2C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C19	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A2C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C25	0160-3447	5	6	CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3447
A2C26	0160-3447	5		CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3447
A2C27	0160-3447	5		CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3447
A2C28	0160-3447	5		CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3447
A2C29	0160-3447	5		CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3447
A2C30	0160-2204	0	4	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A2C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2CR1	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A2CR2	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A2CR3	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A2E1	01615-81301	5	5	JUMPER CLIP, DBA	28480	01615-81301
A2J1	1200-0475	0	9	CONNECTOR-SGL CONT SKT .016-IN-BSC-SZ	28480	1200-0475
A2R1	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R2	0757-0429	2	2	RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A2R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R5	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2R6	0757-0410	1	20	RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R7	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R8	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R9	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R10	2100-3351	6	7	RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A2R11	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A2R12	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A2R13	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A2R14	0757-0407	6	11	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R15	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R16	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R17	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R18	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R19	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R20	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R21	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R22	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A2R23	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A2R24	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A2R25	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R26	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R27	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R28	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R29	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R30	0757-0419	0	5	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A2R31	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A2R34	0757-0416	7	7	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A2R35	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A2R36	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A2R37	0698-0082	7	3	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A2R38	0698-0084	9	3	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R39	0698-3151	7	3	RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A2R40	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A2R41	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A2R42	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A2R43	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R44	0757-0414	5	3	RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
A2R45	0757-0421	4	1	RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A2R46	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R47	0757-0394	0	4	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A2R48	0757-0346	2	4	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A2R49	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A2R51	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A2R52	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R53	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R54	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A2R55	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A2R56	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A2R57	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A2R58	0757-0403	2	2	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A2R59	0757-0403	2		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A2R60	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A2R61	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R62	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R63	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R64	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R65	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R66	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R67	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R68	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R69	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R70	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2TP1	1251-2229	3	4	CONNECTOR-SGL CONT SKT .033-IN-BSC-SZ	28480	1251-2229
	1251-4045	5	4	SOCKET-GROUND SPRING STEEL, 0.190 IN ID	28480	1251-4045
A2TP2	1251-2229	3		CONNECTOR-SGL CONT SKT .033-IN-BSC-SZ	28480	1251-2229
	1251-4045	5		SOCKET-GROUND SPRING STEEL, 0.190 IN ID	28480	1251-4045
A2TP3	1251-2229	3		CONNECTOR-SGL CONT SKT .033-IN-BSC-SZ	28480	1251-2229
	1251-4045	5		SOCKET-GROUND SPRING STEEL, 0.190 IN ID	28480	1251-4045
A2TP4	1251-2229	3		CONNECTOR-SGL CONT SKT .033-IN-BSC-SZ	28480	1251-2229
	1251-4045	5		SOCKET-GROUND SPRING STEEL, 0.190 IN ID	28480	1251-4045
A2TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2U1	1820-0809	8		IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A2U2	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A2U3	1820-1433	6	9	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A2U4	1820-1217	4	2	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS151N
A2U5	1820-1991	1	3	IC CNTR TTL LS DECD DUAL 4-BIT	01295	SN74LS390N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2U6	1820-1991	1		IC CNTR TTL LS DECD DUAL 4-BIT	01295	SN74LS390N
A2U7	1820-1991	1		IC CNTR TTL LS DECD DUAL 4-BIT	01295	SN74LS390N
A2U8	1820-0686	9	2	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A2U9	1820-1475	6		IC CNTR TTL S BIN SYNCHRD POS-EDGE-TRIG	07263	93S16DC
A2U10	1820-1430	3	20	IC CNTR TTL LS BIN SYNCHRD POS-EDGE-TRIG	01295	SN74LS161AN
A2U11	1820-1430	3		IC CNTR TTL LS BIN SYNCHRD POS-EDGE-TRIG	01295	SN74LS161AN
A2U12	1820-1430	3		IC CNTR TTL LS BIN SYNCHRD POS-EDGE-TRIG	01295	SN74LS161AN
A2U13	1820-1475	6		IC CNTR TTL S BIN SYNCHRD POS-EDGE-TRIG	07263	93S16DC
A2U14	1820-1225	4	3	IC FF ECL D-M/S DUAL	04713	MC10231P
A2U15	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A2U16	1820-2010	7		IC	28480	1820-2010
A2U17	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
A2U18	1820-1992	2	1	IC CNTR TTL LS DECD 4-BIT	34335	AM25LS160PC
A2U19	1820-1158	2	3	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
A2U20	1820-0693	8	7	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A2U21	1820-0691	6	12	IC GATE TTL S AND-OR-INV	01295	SN74S64N
A2U22	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A2U23	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A2U24	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A2U25	1820-1730	6	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U26	1820-0817	8	6	IC FF ECL D-M/S DUAL	04713	MC10131P
A2U27	1820-2010	7		IC	28480	1820-2010
A2U28	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A2U29	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A2U30	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A2U31	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A2U32	1820-1074	1	2	IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A2U33	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
A2U34	1820-1372	2		IC FF TTL S J-K BAR CLEAR DUAL	07263	74S109DC
A2U35	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A2U36	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A2U37	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A2U38	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A2U39	1820-1831	8	1	IC GATE ECL OR QUAD 2-INP	04713	MC10103L
A2U40	1820-1946	6	2	IC GATE ECL DUAL	04713	MC10117L
A2U41	1820-1320	0	1	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10216L
A2U42	1820-0808	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A2U43	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A2U44	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A2U45	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A2U46	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A2U47	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A2U48	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A2U49	1820-0682	5	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S03N
A2U50	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A2U51	1820-1201	6	3	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A2U52	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A2U53	1820-1918	2	4	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A2U54	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A2U55	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A2U56	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A2U57	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A2VR1	1902-3070	5	2	DIODE-ZNR 4.22V 5% DO-7 PD=.4W TC=-.038%	28480	1902-3070
A2VR2	1902-3070	5		DIODE-ZNR 4.22V 5% DO-7 PD=.4W TC=-.038%	28480	1902-3070
A2XU14	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A2XU15	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A2XU26	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A2Y1	0410-1032	1	1	CRYSTAL-QUARTZ 20.00000 MHZ	28480	0410-1032
A3	01615-66503	7	1	BOARD ASSEMBLY, MEMORY	28480	01615-66503
A3C1	0160-2200	6		CAPACITOR-FXD 43PF +-5% 300VDC MICA	28480	0160-2200
A3C2	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A3C3	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A3C4	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C5	0160-3802	6	1	CAPACITOR-FXD 150PF +-10% 100VDC CER	28480	0160-3802
A3C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3E1	01615-81301	5		JUMPER CLIP, OSA	28480	01615-81301
A3E2	01615-81301	5		JUMPER CLIP, OSA	28480	01615-81301
A3J1	1200-0475	0		CONNECTOR-SGL CONT SKT .016-IN-BSC-SZ	28480	1200-0475
A3R1	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A3R2	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3R3	0684-4711	8	2	RESISTOR 470 10% .25W FC TC=-400/+600	01121	CB4711
A3R4	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A3R5	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A3R6	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A3R7	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A3R8	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A3R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R13	0684-4711	8		RESISTOR 470 10% .25W FC TC=-400/+600	01121	CB4711
A3R14	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R15	0698-3381	5	1	RESISTOR 150 5% .125W CC TC=-330/+800	01121	BB1515
A3R16	0757-0395	1	1	RESISTOR 56.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-56R2-F
A3R17	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R20	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R21	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R22	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R23	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R24	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R25	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A3TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3U1	1816-1092	4		IC MEMORY	28480	1816-1092
A3U2	1816-1092	4		IC MEMORY	28480	1816-1092
A3U3	1816-1092	4		IC MEMORY	28480	1816-1092
A3U4	1816-1092	4		IC MEMORY	28480	1816-1092
A3U5	1820-1210	7	4	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A3U6	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U7	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
A3U8	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A3U9	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A3U10	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A3U11	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A3U12	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A3U13	1816-1092	4		IC MEMORY	28480	1816-1092
A3U14	1816-1092	4		IC MEMORY	28480	1816-1092
A3U15	1816-1092	4		IC MEMORY	28480	1816-1092
A3U16	1816-1092	4			28480	1816-1092
A3U17	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A3U18	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
A3U19	1820-1372	2		IC FF TTL S J-K BAR CLEAR DUAL	07263	74S109DC
A3U20	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A3U21	1820-1074	1		IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A3U22	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A3U23	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A3U24	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A3U25	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A3U26	1816-1092	4		IC MEMORY	28480	1816-1092
A3U27	1816-1092	4		IC MEMORY	28480	1816-1092
A3U28	1816-1092	4		IC MEMORY	28480	1816-1092
A3U29	1816-1092	4		IC MEMORY	28480	1816-1092
A3U30	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A3U31	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A3U32	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A3U33	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U34	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U35	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U36	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U37	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A3U38	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A3U39	1816-1092	4		IC MEMORY	28480	1816-1092
A3U40	1816-1092	4		IC MEMORY	28480	1816-1092
A3U41	1816-1092	4		IC MEMORY	28480	1816-1092
A3U42	1816-1092	4		IC MEMORY	28480	1816-1092
A3U43	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A3U44	1820-1435	8	2	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N
A3U45	1820-1435	8		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U46	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A3U47	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A3U48	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U49	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U50	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U51	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A4	01615-66504	8	1	BOARD ASSEMBLY, TIMING DATA ACQ.	28480	01615-66504
A4C1	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A4C2	0140-0206	6	2	CAPACITOR-FXD 270PF +-5% 500VDC MICA	72136	DM15F271J0500WV1CR
A4C3	0140-0208	8	1	CAPACITOR-FXD 680PF +-5% 300VDC MICA	72136	DM15F681J0300WV1CR
A4C4	0160-4625	3	1	CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4625
A4C5	0160-4623	1	1	CAPACITOR-FXD 3900PF +-5% 100VDC CER	28480	0160-4623
A4C6	0160-4624	2	1	CAPACITOR-FXD 8200PF +-5% 50VDC CER	28480	0160-4624
A4C7	0160-4696	8	1	CAPACITOR-FXD .018UF +-5% 50VDC	28480	0160-4696
A4C8	0140-0190	7	2	CAPACITOR-FXD 39PF +-5% 300VDC MICA	72136	DM15E390J0300WV1CR
A4C9	0140-0190	7		CAPACITOR-FXD 39PF +-5% 300VDC MICA	72136	DM15E390J0300WV1CR
A4C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C13	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A4C14	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A4C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4CR1	1901-0040	1	9	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4J1	1251-5055	9	1	CONNECTOR 26-PIN M POST TYPE	08261	801-079
A4R1	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A4R2	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A4R3	0683-0475	1	3	RESISTOR 4.7 5% .25W FC TC=-400/+500	01121	CB47G5
A4R4	0757-0399	5	2	RESISTOR 82.5 1% .125W F TC=0+-100	24546	C4-1/8-T0-82R5-F
A4R5	0757-0399	5		RESISTOR 82.5 1% .125W F TC=0+-100	24546	C4-1/8-T0-82R5-F
A4R6	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A4R7	0757-0411	2	1	RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-T0-332R-F
A4R8	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A4R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R10	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R11	0683-0475	1		RESISTOR 4.7 5% .25W FC TC=-400/+500	01121	CB47G5
A4R12	0683-0475	1		RESISTOR 4.7 5% .25W FC TC=-400/+500	01121	CB47G5
A4R13	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A4R14	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R15	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R16	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R17	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A4R18	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R19	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R20	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A4R21	0757-0282	5		RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A4R22	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R23	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R24	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R25	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R26	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R27	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R28	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R29	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R30	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R31	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R32	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4U1	1820-0810	1	3	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A4U2	1816-1335	8		IC TTL S 256-BIT RAM 11-NS	04713	MCM10152L
A4U3	1816-1335	8		IC TTL S 256-BIT RAM 11-NS	04713	MCM10152L
A4U4	1820-1482	5	1	IC GATE ECL NOR DUAL 3-INP	04713	MC10211P
A4U5	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A4U6	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A4U7	1820-0801	0	1	IC GATE ECL OR-NOR QUAD 2-INP	04713	MC10101P
A4U8	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U9	1820-0820	3	16	IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U10	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U11	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U12	1820-1990	0	4	IC GATE ECL NOR QUAD 2-INP	04713	MC10100L
A4U13	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U14	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U15	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U16	1820-0810	1		IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A4U17	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A4U18	1820-1993	3	2	IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158L
A4U19	1820-0684	7	1	IC INV TTL S HEX 1-INP	01295	SN74S05N
A4U20	1820-2010	7		IC	28480	1820-2010
A4U21	1820-2010	7		IC	28480	1820-2010
A4U22	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U23	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U24	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A4U25	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U26	1820-1990	0		IC GATE ECL NOR QUAD 2-INP	04713	MC10100L
A4U27	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U28	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A4U29	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U30	1820-0810	1		IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A4U31	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A4U32	1820-1993	3		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158L
A4U33	1820-2010	7		IC	28480	1820-2010
A4U34	1820-2010	7		IC	28480	1820-2010
A4U35	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U36	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U37	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U38	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U39	1820-1990	0		IC GATE ECL NOR QUAD 2-INP	04713	MC10100L
A4U40	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U41	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U42	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U43	1820-1946	6		IC GATE ECL DUAL	04713	MC10117L
A4U44	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U45	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A4U46	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A4U47	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U48	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U49	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A4U50	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U51	1820-1990	0		IC GATE ECL NOR QUAD 2-INP	04713	MC10100L
A4U52	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U53	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A4U54	1820-0820	3		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135L
A4U55	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U56	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U57	1810-0272	8	3	NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4U58	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U59	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U60	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U61	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U62	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U63	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U64	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4U65	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4U66	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U67	1810-0302	5	6	NETWORK-RES 8-SIP47.0 OHM X 4	01121	208B470
A4U68	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208B470
A4U69	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208B470
A4U70	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208B470
A4U71	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208B470
A4U72	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208B470
A4U73	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U74	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4U75	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4U76	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A4XU2	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A4XU5	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A4XU8	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A4XU22	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A4XU35	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A4XU44	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A4XU47	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A5	01615-66517	1	1	BOARD ASSEMBLY, MICROPROCESSOR AND ROM	28480	01615-66517
A5C1	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A5C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A5C5	0180-0197	8	2	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A5C8	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A5C9	0170-0066	9	1	CAPACITOR-FXD .027UF +-10% 200VDC POLYE	28480	0170-0066
A5C12	0140-0206	6		CAPACITOR-FXD 270PF +-5% 500VDC MICA	72136	DM15F2T1J0500WV1CR
A5C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C31	0160-2201	7	1	CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A5CR1	1901-0025	2	2	DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5CR2	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5E1	01615-81301	5		JUMPER CLIP, OSA	28480	01615-81301
A5J1	1251-4524	5	1	CONNECTOR 20-PIN M POST TYPE	28480	1251-4524
A5J2	1200-0475	0		CONNECTOR-SGL CONT SKT .016-IN-BSC-SZ	28480	1200-0475
A5Q1	1854-0215	1	7	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A5Q2	1853-0016	8	1	TRANSISTOR PNP SI TO-92 PD=300MW	28480	1853-0016
A5R1	0698-3154	0	2	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A5R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R4	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A5R7	0761-0054	8	2	RESISTOR 330 5% 1W MO TC=0+-200	28480	0761-0054
A5R8	0761-0054	8		RESISTOR 330 5% 1W MO TC=0+-200	28480	0761-0054
A5R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R15	0757-0438	3	3	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R16	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R17	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R19	0757-0338	2	1	RESISTOR 1K 1% .25W F TC=0+-100	24546	C5-1/4-T0-1001-F
A5R20	0757-0398	4	1	RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A5R21	0757-0401	0	9	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A5R23	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R24	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A5R26	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5R27	0684-1001	3	1	RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A5R28	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R29	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R30	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R31	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R32	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R33	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R35	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R36	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R37	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R38				DELETED		
A5TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5U1	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A5U2	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
A5U3	1818-0474	8	1	IC NMOS 16384-BIT ROM	27014	DM2316EN MASKED
A5U4	1818-0475	9	1	IC NMOS 16384-BIT ROM	27014	DM2316EN MASKED
A5U5	1818-0473	7	1	IC NMOS 16384-BIT ROM	27014	DM2316EN MASKED
A5U6	1818-0472	6	1	IC NMOS 16384-BIT ROM	27014	DM2316EN MASKED
A5U7	1818-0471	5	1	IC NMOS 16384-BIT ROM	27014	DM2316EN MASKED
A5U8	1818-0470	4	1	IC NMOS 16384-BIT ROM	27014	DM2316EN MASKED
A5U9	1820-1918	2		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A5U10	1820-1918	2		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A5U11	1820-1783	9	1	IC MICPROC NMOS 8-BIT	01295	TMS8080AN
A5U12	1820-1994	4	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS243N
A5U13	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
A5U14	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A5U15	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A5U16	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A5U17	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U18	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A5U20	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A5U21	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A5U22	1820-1641	8	1	IC DRVR TTL LS BUS DRVR HEX 1-INP	01295	SN74LS365AN
A5U23	1820-1918	2		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A5U24	1820-1994	4		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS243N
A5U25	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A5U26	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A5U27	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A5U28	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A5U31	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A5U32	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A5U33	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A5U34	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A5U35	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A5U36	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A5U37	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A5U38	1820-1429	0	2	IC CNTR TTL LS DECD SYNCHRO	01295	SN74LS160AN
A5U39	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A5U40	1820-1204	9	2	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A5U41	1820-1210	7		IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A5U42	1810-0049	7	1	NETWORK-RES 12-SIP6.8K OHM X 10	28480	1810-0049
A5XU3	1200-0541	1	6	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A5XU4	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A5XU5	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A5XU6	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A5XU7	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A5XU8	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A5XU11	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A5XU12	1200-0638	7	3	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0638
A5XU24	1200-0638	7		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0638
A6	01615-66516	2	1	BOARD ASSEMBLY, DISPLAY PROGRAMMER	28480	01615-66516
A6C1	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A6C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A6C3	0160-3447	5		CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3447
A6C4	0160-2205	1	4	CAPACITOR-FXD 120PF +-5% 300VDC MICA	28480	0160-2205
A6C5	0160-2205	1		CAPACITOR-FXD 120PF +-5% 300VDC MICA	28480	0160-2205
A6C6	0160-2205	1		CAPACITOR-FXD 120PF +-5% 300VDC MICA	28480	0160-2205
A6C7	0160-2205	1		CAPACITOR-FXD 120PF +-5% 300VDC MICA	28480	0160-2205
A6C8	0160-0939	4	1	CAPACITOR-FXD 430PF +-5% 300VDC MICA	28480	0160-0939
A6C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6C21	0160-2209	5	1	CAPACITOR-FXD 360PF +-5% 300VDC MICA	28480	0160-2209
A6C22	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A6C23	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A6R1	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A6R2	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R3	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R5	0757-0408	7	1	RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-T0-243R-F
A6R6	0757-0283	6	8	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R7	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R8	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R9	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R10	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R14	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R15	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R16	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R17	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R18	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R19	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R20	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R21	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A6R22	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A6R23	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R24	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R25	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R26	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R27	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R28	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R29	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R30	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R31	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A6R32	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R33	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A6R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R35	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-TO-511R-F
A6R36	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6U1	1818-0237	1	1	IC PMOS 2.5K ROM CHAR GEN 450-NS 3-S	14936	R0-3-2513
A6U2	1820-1042	3	1	IC SHF-RGTR TTL R-S PRL-IN SERIAL-OUT	01295	SN74165N
A6U3	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A6U4	1820-1194	6	3	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
A6U5	1820-1194	6		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
A6U6	1820-1194	6		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
A6U7	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A6U8	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U9	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U10	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U11	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U12	1820-1210	7		IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A6U13	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A6U14	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A6U15	1820-1470	1	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A6U16	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A6U17	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A6U18	1820-0687	0	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S15N
A6U19	1816-0913	6	1	IC TTL S 64-BIT RAM 110-NS O-C	34335	AM31L01PC
A6U20	1820-1217	4		IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS151N
A6U21	1820-1298	1	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS251N
A6U22	1816-1149	2	1	IC TTL S 1K ROM 65-NS 3-S	01295	SN74S287N PROGRAMMED
A6U23	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U24	1820-1204	9		IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A6U25	1820-1202	7	2	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A6U26	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A6U27	1820-1192	4	2	IC RGTR TTL D-TYPE 4-BIT	01295	SN74173N
A6U28	1818-0348	5	8	IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U29	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U30	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6U31	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U32	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U33	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A6U34	1816-1148	1	1	IC TTL S 1K ROM 65-NS 3-S	01295	SN74S287N PROGRAMMED
A6U35	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A6U36	1816-1150	5	1	IC TTL S 1K ROM 65-NS 3-S	01295	SN74S287N PROGRAMMED
A6U37	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U38	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U39	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U40	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A6U41	1820-1192	4		IC RGTR TTL D-TYPE 4-BIT	01295	SN74173N
A6U42	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U43	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U44	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U45	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U46	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A6U47	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A6U48	1820-1210	7		IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A6U49	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A6U50	1816-1151	6	1	IC TTL S 1K ROM 65-NS 3-S	01295	SN74S287N PROGRAMMED
A6U51	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U52	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A6U53	1820-1429	0		IC CNTR TTL LS DECD SYNCHRO	01295	SN74LS160AN
A6XU15	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A6XU22	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A6XU23	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A6XU34	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A6XU36	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A6XU50	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A6XU51	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
A6XU52	1200-0638	7		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0638
A7	01615-66513	9	1	BOARD ASSEMBLY, POWER SUPPLY	28480	01615-66513
A7C1	0180-0230	0	8	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A7C2	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A7C3	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A7C4	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A7C5	0180-0116	1	2	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A7C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C7	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A7C8	0160-2197	0	1	CAPACITOR-FXD 10PF +-5% 300VDC MICA	28480	0160-2197
A7C9	0180-2750	3	2	CAPACITOR-FXD 3300UF+100-10% 6.3VDC AL	56289	672D338H6R3JE2C
A7C10	0160-0161	4	3	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A7C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C12	0160-3508	9	7	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A7C13	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A7C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C15	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A7C16	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A7C17	0160-0161	4		CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A7C18	0180-2750	3		CAPACITOR-FXD 3300UF+100-10% 6.3VDC AL	56289	672D338H6R3JE2C
A7C19	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A7C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C21	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A7C22	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A7CR1	1901-0662	3	6	DIODE-PWR RECT 100V 6A	04713	MR751
A7CR2	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A7CR3	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A7CR4	1901-0511	1	1	DIODE-PWR RECT 1N3889R 50V 12A 200NS	04713	1N3889R
A7CR5	1884-0266	5	1	THYRISTOR-SCR 2N6400 TO-220AB VRRM=50	01928	2N6400
A7CR6	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A7CR7	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A7CR8	1901-0791	9	1	DIODE-PWR RECT 1N3889 50V 12A 200NS DO-4	55967	1N3889
A7CR9	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A7CR10	1884-0276	7	1	THYRISTOR-TRIAC TO-220AB	28480	1884-0276
A7CR11	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A7DS1	2140-0493	5	1	LAMP-INCAND 55 7VDC 41MA G-4 1/2-BULB	08806	55
A7E1	0360-1758	7	2	CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1758
A7F1	2110-0002	8	2	RESISTOR-VAR CONTROL WW 50 10% LIN	28480	2100-0002
A7F2	2110-0002	5		RESISTOR-VAR CONTROL WW 50 10% LIN	28480	2100-0002
A7F3	2110-0528	4	2	FUSE 10A 125V FAST-BLO 1.25X.25 UL	75915	312010
A7F4	2110-0528	4		FUSE 10A 125V FAST-BLO 1.25X.25 UL	75915	312010

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7H1	2360-0195	0	4	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A7H2	2420-0001	5	9	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A7H3	2740-0003	5	2	NUT-HEX-W/LKWR 10-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
A7L1	9140-0242	9	2	COIL 100UH 10% .9370X1.625LG-NOM	28480	9140-0242
A7L2	9140-0242	9		COIL 100UH 10% .9370X1.625LG-NOM	28480	9140-0242
A7MP1	0380-0327	0	2	SPACER-RND .125-IN-LG .09-IN-ID	28480	0380-0327
A7MP1	1205-0310	2	5	HEAT SINK SGL TO-3-CS	28480	1205-0310
A7MP2	1400-0493	6	2	CABLE TIE .062-1.25-DIA .14-WD NYL	28480	1400-0493
A7Q1	1853-0084	0	1	TRANSISTOR PNP 2N4918 SI PD=30W FT=3MHZ	04713	2N4918
A7Q2	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A7Q3	1854-0300	5	1	TRANSISTOR NPN SI PD=25W FT=4MHZ	28480	1854-0300
A7Q4	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7R1	0757-0479	2	1	RESISTOR 392K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-3923-F
A7R2	0684-6811	3	2	RESISTOR 680 10% .25W FC TC=-400/+600	01121	CB6811
A7R3	0757-0473	6	1	RESISTOR 221K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2213-F
A7R4	0683-1505	0	1	RESISTOR 15 5% .25W FC TC=-400/+500	01121	CB1505
A7R5	0687-2201	3	2	RESISTOR 22 10% .5W CC TC=0+412	01121	EB2201
A7R6	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R7	0757-0414	5		RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
A7R8	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A7R9	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A7R10	0683-1205	7	2	RESISTOR 12 5% .25W FC TC=-400/+500	01121	CB1205
A7R11	0757-0278	9	5	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A7R12	2100-3352	7	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A7R13	0811-1758	8	8	RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A7R14	0811-1758	8		RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A7R15	0811-1758	8		RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A7R16	0683-0275	9	4	RESISTOR 2.7 5% .25W FC TC=-400/+500	01121	CB27G5
A7R17	0683-0685	5	1	RESISTOR 6.8 5% .25W FC TC=-400/+500	01121	CB68G5
A7R18	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A7R19	0683-0275	9		RESISTOR 2.7 5% .25W FC TC=-400/+500	01121	CB27G5
A7R20	0684-5601	7	2	RESISTOR 56 10% .25W FC TC=-400/+500	01121	CB5601
A7R21	0683-3025	3	1	RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A7R22	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A7R23	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A7R24	0683-5125	8	1	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A7R25	0687-2201	3		RESISTOR 22 10% .5W CC TC=0+412	01121	EB2201
A7R26	0698-3150	6	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A7R27	0683-1015	7	1	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A7R28	0683-0275	9		RESISTOR 2.7 5% .25W FC TC=-400/+500	01121	CB27G5
A7R29	0683-1205	7		RESISTOR 12 5% .25W FC TC=-400/+500	01121	CB1205
A7R30	0684-3921	0	3	RESISTOR 3.9K 10% .25W FC TC=-400/+700	01121	CB3921
A7R31	0684-6811	3		RESISTOR 680 10% .25W FC TC=-400/+600	01121	CB6811
A7R32	0757-0414	5		RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
A7R33	0811-1758	8		RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A7R34	0811-1758	8		RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A7R35	0811-1758	8		RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A7R36	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R37	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R38	0683-0275	9		RESISTOR 2.7 5% .25W FC TC=-400/+500	01121	CB27G5
A7R39	0684-5601	7		RESISTOR 56 10% .25W FC TC=-400/+500	01121	CB5601
A7R40	0811-1758	8		RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A7R41	0811-1758	8		RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A7TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7U1	1820-0439	0	1	IC V RGLTR 14-DIP-P	07263	723PC
A7U2	1826-0004	7	1	IC 304 V RGLTR TO-100	07263	UA304HC
A7VR1	1902-3104	6	2	DIODE-ZNR 5.62V 5% DO-7 PD=.4W TC=+.016%	28480	1902-3104
A7VR2	1902-3104	6		DIODE-ZNR 5.62V 5% DO-7 PD=.4W TC=+.016%	28480	1902-3104
A7XDS1	1450-0584	1	1	LAMP SOCKET MINTR-BAY-SKT	95263	7-35XP11
A7XF1	2110-0269	0	8	FUSEHOLDER-CLIP TYPE.250-FUSE	28480	2110-0269
A7XF2	2110-0269	0		FUSEHOLDER-CLIP TYPE.250-FUSE	28480	2110-0269
A7XF3	2110-0269	0		FUSEHOLDER-CLIP TYPE.250-FUSE	28480	2110-0269
A7XF4	2110-0269	0		FUSEHOLDER-CLIP TYPE.250-FUSE	28480	2110-0269
A8	01615-66508	2	1	BOARD ASSEMBLY, MOTHER	28480	01615-66508

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8C1	0180-2770	7	2	CAPACITOR-FXD .018F+75-10% 30VDC AL	28480	0180-2770
A8C2	0180-2770	7		CAPACITOR-FXD .018F+75-10% 30VDC AL	28480	0180-2770
A8E1	0360-1653	5	4	CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A8E2	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A8E3	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A8E4	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A8J1	1251-3195	4	2	CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
A8J2	1251-3276	2	1	CONNECTOR 6-PIN M POST TYPE	28480	1251-3276
A8J3	1251-3195	4		CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
A8MP1	0380-0059	5	2	SPACER-RVT-ON .25-IN-LG .152-IN-ID	00000	ORDER BY DESCRIPTION
A8R1	0684-3921	0		RESISTOR 3.9K 10% .25W FC TC=-400/+700	01121	CB3921
A8R2	0684-3921	0		RESISTOR 3.9K 10% .25W FC TC=-400/+700	01121	CB3921
A8R3	0698-3180	2	1	RESISTOR 68 2% 2W MO TC=0+-200	28480	0698-3180
A8R4	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A8XA1	1251-4587	0	7	CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A8XA2	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A8XA3	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A8XA4	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A8XA5	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A8XA6	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A8XA7	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A8XA9	1251-4547	2	1	CONNECTOR 20-PIN M POST TYPE	28480	1251-4547
A8XA13	1251-1886	6	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	28480	1251-1886
A9	01615-66509	3	1	BOARD ASSEMBLY, PROBE THRESHOLD/INPUT	28480	01615-66509
A9C1	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A9C2	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A9C3	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A9C4	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A9C5	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A9CR1	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A9CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A9L1	9140-0158	6	1	COIL-MLD 1UH 10% Q=32 .095DX.25LG-NOM	28480	9140-0158
A9R1	0757-0278	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A9R2	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A9R3	2100-3588	1	3	RESISTOR-TRMR 10K 20% CCP TOP-ADJ 1-TRN	28480	2100-3588
A9R4	0757-0278	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A9R5	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A9R6	2100-3588	1		RESISTOR-TRMR 10K 20% CCP TOP-ADJ 1-TRN	28480	2100-3588
A9R7	0757-0278	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A9R8	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A9R9	2100-3588	1		RESISTOR-TRMR 10K 20% CCP TOP-ADJ 1-TRN	28480	2100-3588
A9R10	0757-0278	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A9R11	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A9R12	0684-0271	7	2	RESISTOR 2.7 10% .25W FC TC=-400/+500	01121	CB27G1
A9R13	0684-0271	7		RESISTOR 2.7 10% .25W FC TC=-400/+500	01121	CB27G1
A9S1	3101-2118	4	3	SWITCH-TGL SUBMIN SPDT 5A 120VAC	28480	3101-2118
A9S2	3101-2118	4		SWITCH-TGL SUBMIN SPDT 5A 120VAC	28480	3101-2118
A9S3	3101-2118	4		SWITCH-TGL SUBMIN SPDT 5A 120VAC	28480	3101-2118
A9W1	01615-61607	2	1	CABLE ASSEMBLY, INTERCONNECT FOR A9	28480	01615-61607
A10	01615-66510	6	1	BOARD ASSEMBLY, KEYBOARD	28480	01615-66510
A10C1	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X901082
A10C3	0160-3622	8	3	CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A10C4	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A10C5	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A10C6	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A10C7	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A10C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10C10	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A10C11	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A10E1	0360-1788	7		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1788
A10MP1	2360-0115	4	36	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10MP2	0380-0585	2	3	STANDOFF-RVT-ON .531-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
A10MP3	01615-04701	7	1	SUPPORT, KEYSWITCH,SHEET METAL PLATE	28480	01615-04701
A10R1	0757-0400	9	2	RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A10R2	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A10R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R4	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A10R5	0684-1031	9	1	RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10R6	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A10R7	0757-0273	4	1	RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A10R8	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R10	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A10R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R12	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A10R13	0757-0400	9		RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A10S1- A10S36	3101-2137	7	43	SWITCH-PB SPST-NO MOM	28480	3101-2137
A10U1	1820-0491	4	1	IC DCDR TTL BCD-TO-DEC 4-TO-10-LINE	01295	SN74145N
A10U2	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
A10U3	1821-0002	5	1	TRANSISTOR ARRAY	01928	CA3045
A10W1	01615-61606	1	1	CABLE ASSEMBLY, KEYBOARD	28480	01615-61606
A12	01615-66512	8	1	BOARD ASSEMBLY, EXTENDER	28480	01615-66512
A13	01611-66503	3	2	BOARD ASSEMBLY, DISPLAY DRIVER	28480	01611-66503
A13C1	0160-0161	4		CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A13C2	0140-0199	6	1	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A13C3	0180-0097	7	6	CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X9035S2
A13C4	0180-0106	9	3	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A13C5	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X9035B2
A13C6	0160-4455	7	1	CAPACITOR-FXD 10UF +-10% 50VDC MET-POLYC	28480	0160-4455
A13C7	0160-3127	8	2	CAPACITOR-FXD .022UF +-5% 400VDC POLYE	84411	663UW22354W2
A13C8	0160-3830	0	1	CAPACITOR-FXD 5UF +-10% 50VDC MET-POLYC	28480	0160-3830
A13C9	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A13C10	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A13C11	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A13C12	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A13C13	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A13C14	0160-3762	7	2	CAPACITOR-FXD .68UF +-5% 50VDC MET-POLYC	28480	0160-3762
A13C15	0160-3762	7		CAPACITOR-FXD .68UF +-5% 50VDC MET-POLYC	28480	0160-3762
A13C16	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X9035B2
A13C17	0180-1819	3	1	CAPACITOR-FXD 100UF+75-10% 50VDC AL	56289	30D107G050DH2
A13C18	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X9035S2
A13C19	0160-3127	8		CAPACITOR-FXD .022UF +-5% 400VDC POLYE	84411	663UW22354W2
A13C20	0180-2667	1	1	CAPACITOR-FXD 150UF+-10% 20VDC TA	56289	150D157X9020B2
A13C21	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A13C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A13C23	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A13C24	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A13C25	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X9035B2
A13C26	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X9035B2
A13C27	0160-4449	9	1	CAPACITOR-FXD 8200PF +-10% 400VDC POLYE	28480	0160-4449
A13C28	0160-3665	9	6	CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A13C29	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A13C30	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A13C31	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A13C32	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A13C33	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A13C34	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A13C35	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A13C36	0180-0098	8	1	CAPACITOR-FXD 100UF+-20% 20VDC TA	56289	150D107X0020B2
A13C37	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A13CR1	1901-0767	9	3	DIODE-PWR RECT 400V 6A	04713	7 754
A13CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13CR3	1901-0029	6	5	DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A13CR4	1901-0767	9		DIODE-PWR RECT 400V 6A	04713	7 754
A13CR5	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A13CR6	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A13CR7	1901-0767	9		DIODE-PWR RECT 400V 6A	04713	7 754
A13CR8	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A13CR9	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A13H1	2360-0201	9	6	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A13H2	2420-0003	7	6	NUT-HEX-DBL-CHAM 6-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A13H3	2260-0001	5	2	NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
A13H4	2190-0018	5	6	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0018
A13H5	2190-0019	6	6	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
A13H6	3050-0016	8	6	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0016
A13H7	3050-0235	3	6	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13L1	9100-3930	4	1	COIL 2.5MH 10% .625DX1.437LG-NOM	28480	9100-3930
A13L2	9100-3877	8	1	COIL-MLO 290MM SRF=1KHZ	28480	9100-3877
A13L3	9100-3931	5	1	COIL 700UH 10% .6DX1.437LG-NOM	28480	9100-3931
A13L4	01611-86001	8	1	INDUCTOR, FXO 0.6 UH	28480	01611-86001
A13L5	9140-0111	1	1	COIL-MLO 3.3UH 10% Q=33 .155DX.375LG-NOM	28480	9140-0111
A13MP1	1205-0310	2		HEAT SINK SGL TO-3-CS	28480	1205-0310
A13MP2	0380-0384	9	3	STANOOFF-RVT-ON 1.25-IN-LG 6-32THD	28480	0380-0384
A13MP3	1400-0249	0	2	CABLE TIE .062-.625-DIA .091-WD NYL	28480	1400-0249
A13Q1	1854-0751	0	3	TRANSISTOR NPN 2N5840 SI TO-3 PD=100W	07263	2N5840
A13Q2	1854-0558	5	1	TRANSISTOR NPN SI DARL PD=70W FT=1MHZ	28480	1854-0558
A13Q3	1853-0334	3	1	TRANSISTOR PNP SI DARL PD=70W FT=1MHZ	04713	MJE1090
A13Q4	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A13Q5	1854-0330	1	1	TRANSISTOR NPN SI PD=21W FT=10MHZ	28480	1854-0330
A13Q6	1854-0751	0		TRANSISTOR NPN 2N5840 SI TO-3 PD=100W	07263	2N5840
A13Q7	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A13Q8	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A13Q9	1854-0751	0		TRANSISTOR NPN 2N5840 SI TO-3 PD=100W	07263	2N5840
A13Q10	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A13Q11	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A13Q12	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A13Q13	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A13R1	0757-0812	7	1	RESISTOR 432 1% .5W F TC=0+-100	28480	0757-0812
A13R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A13R3	0811-1678	1	2	RESISTOR 10 5% 2W PW TC=0+-400	75042	BWH2-10R-J
A13R4	0698-3605	6	1	RESISTOR 15 5% 2W MO TC=0+-200	27167	FP42-2-T00-15R0-J
A13R5	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A13R6	2100-3576	7	1	RESISTOR-VAR CONTROL CC 50 10% LIN	01121	73M4G0248500U
A13R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A13R8	0757-0457	6	9	RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R9	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R10	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R11	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R12	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A13R13	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A13R14	2100-3252	6	4	RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
A13R15	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A13R16	0757-0437	2	3	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A13R17	0757-0488	3	3	RESISTOR 909K 1% .125W F TC=0+-100	28480	0757-0488
A13R18	2100-3213	9	1	RESISTOR-TRMR 200K 10% C TOP-ADJ 1-TRN	28480	2100-3213
A13R19	0757-0470	3	2	RESISTOR 162K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1623-F
A13R20	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A13R21	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A13R22	0757-0470	3		RESISTOR 162K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1623-F
A13R23	2100-3252	6		RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
A13R24	0698-5437	6	2	RESISTOR 12K .1% .125W F TC=0+-50	28480	0698-5437
A13R25	0698-5437	6		RESISTOR 12K .1% .125W F TC=0+-50	28480	0698-5437
A13R26	0698-5420	7	2	RESISTOR 3.874K .1% .125W F TC=0+-50	28480	0698-5420
A13R27	0698-5420	7		RESISTOR 3.874K .1% .125W F TC=0+-50	28480	0698-5420
A13R28	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A13R29	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A13R30	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A13R31	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A13R32	0811-1671	4	1	RESISTOR 2.7 5% 2W PW TC=0+-400	75042	BWH2-2R7-J
A13R33	0757-0804	7	1	RESISTOR 200 1% .5W F TC=0+-100	28480	0757-0804
A13R34	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A13R35	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R36	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R37	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R38	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R39	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A13R40	2100-3252	6		RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
A13R41	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A13R42	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A13R43	0811-1678	1		RESISTOR 10 5% 2W PW TC=0+-400	75042	BWH2-10R-J
A13R44	0684-1041	1	2	RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
A13R45	2100-0569	2	1	RESISTOR-TRMR 1M 20% C TOP-ADJ 1-TRN	28480	2100-0569
A13R46	0684-1041	1		RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
A13R47	0757-0488	3		RESISTOR 909K 1% .125W F TC=0+-100	28480	0757-0488
A13R48	0757-0488	3		RESISTOR 909K 1% .125W F TC=0+-100	28480	0757-0488
A13R49	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A13R50	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A13R51	0757-0159	5	2	RESISTOR 1K 1% .5W F TC=0+-100	28480	0757-0159
A13R52	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A13R53	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A13R54	0698-0090	7	1	RESISTOR 464 1% .5W F TC=0+-100	28480	0698-0090
A13R55	0757-0412	3	1	RESISTOR 365 1% .125W F TC=0+-100	24546	C4-1/8-T0-365R-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13R56	0T5T-0284	T		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A13R5T	0757-0469	0	1	RESISTOR 150K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1503-F
A13R58	0757-0453	2	1	RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
A13R59	0T57-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A13R60	2100-3214	0	1	RESISTOR-TRMR 100K 10% C TOP-AOJ 1-TRN	28480	2100-3214
A13R61	2100-3252	6		RESISTOR-TRMR 5K 10% C TOP-AOJ 1-TRN	28480	2100-3252
A13R62	0T57-0159	5		RESISTOR 1K 1% .5W F TC=0+-100	28480	0T5T-0159
A13T1	5061-1228	1	1		28480	5061-1228
A13T2	9100-3927	9	1	TRANSFORMER FLYBACK	28480	9100-3927
A13TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TP4	0360-0535	0		TERMINAL TEST POIN7 PCB	00000	ORDER BY DESCRIPTION
A13TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TR6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TR7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TR10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13TP11	0360-0535	0		TERMINAL TEST ROINT PCB	00000	ORDER BY DESCRIPTION
A13TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A13U1	1826-0254	9	4	IC OP AMP GP 8-DIP-P	04T13	MC1T418CP1
A13U2	1826-0254	9		IC OR AMP OR 8-DIP-P	04T13	MC17418CP1
A13U3	1826-0254	9		IC OP AMP GP 8-DIP-P	04713	MC1T418CP1
A13U4	1826-0254	9		IC OP AMR GP 8-DIR-P	04T13	MC1T418CP1
A13U5	1820-1422	3	1	IC MV TTL LS MONOSTBL RETRIG	01295	SNT4LS122N
A13U6	1820-1796	4	1	IC DRVR TTL DUAL 2-INP	27014	DS3611N
A13VR1	1902-0041	4	1	DIODE-ZNR 5.11V 5% DO-T PD=.4W TC=-.009%	28480	1902-0041
A13VR2	1902-0593	1	1	DIODE-ZNR 43.2V 10% DO-15 PD=1W TC=+.08%	28480	1902-0593

Table 6-2. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMRNT DIV	DALLAS	TX	T5222
01928	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	088T6
04T13	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
0653A	ETRI INC	BURR RIDGE	IL	60521
0T263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
08261	SPECTRA-STRIP CORP	GARDEN GROVE	CA	92642
08806	GE CO MINIATURE LAMP PROD DEPT	CLEVELAND	OH	44112
14936	GENERAL INSTR CORP SEMICON PROD GR	HICKSVILLE	NY	11802
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	T606T
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16T01
26654	VARADYNE INC	SANTA MONICA	CA	90404
2T014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
2T167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
2TTTT	VARO SEMICONDUCTOR INC	GARLAND	TX	T5040
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
5596T	FMC SEMICONDUCTOR PRODUCTS OPER	BROOMFIELD	CO	80020
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	0124T
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108
75915	LITTELFUSE INC	DES PLAINES	IL	60016
84411	TRW CAPACITOR DIV	OGALLALA	NE	69153
95263	LEECRAFT MFG CO INC	LI CITY	NY	11101
9598T	WECKESSER CO INC	CHICAGO	IL	60641

See introduction to this section for ordering information
*Indicates factory selected value

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific instrument.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the serial prefix shown on the manual title page. If the serial prefix of your instrument is not the same as the one on the title page, find your serial prefix in table 7-1 and make the changes to the manual that are listed for that serial prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1, 2, and 3 are required for your serial prefix, do change 3 first, then change 2, and finally change 1.

7-5. If the serial prefix of your instrument is not listed either on the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Manual Changes

Serial Prefix	Make Changes
1742A	5 thru 1
1825A	5 thru 2
1849A	5 thru 3
1905A	4,5
1922A	5

CHANGE 1

Table 6-2,
- A7: Change HP and Mfr Part Nos. to 01615-66507.
- Delete: A7C22.
- A7CR5: Change to HP Part No. 1884-0082, THYR SCR 2N4441.
- A7CR10: Change to HP Part No. 1884-0217, THYRISTOR-TRIAC.
- Delete: A7R40 and A7R41.
- A7VR1: Change to HP Part No. 1902-0041, DZ 5.11 V 5%, 400 MW.

Schematic 2,
- Delete: A7C22, A7R40, and A7R41.
- A7CR5: Change HP Part No. to 1884-0082 and Mfr Part No. to 2N4441.
- A7CR10: Change HP Part No. to 1884-0217 and Mfr Part No. to MAC-10-2.
- A7VR1: Change HP Part No. to 1902-0041, Mfr Part No. to SZ10939-98, and value to 5.11 V.

CHANGE 2

Table 6-2,
- A5: Change HP and Mfr Part Nos. to 01615-66505.
- A5U2: Change to ROM 6 — Not part of standard instrument.
- Add: A5XU2. Same as A5XU8.

Schematic 8A,
- Delete: A5U2.
- Add: A5U2, ROM 6, in parallel with ROM 0 through ROM 5.
- A5U1 pin 9: Connect to ROM 6 pin 20.
- LRAMA: Show supplied by pin 7 of A5U1.
- U25C pin 10: Disconnect from A5U2 pin 7 and connect to LRAMA.

CHANGE 3

Table 6-2,
- Delete: J4.
- MP55: Change HP and Mfr Part Nos. to 01615-00202.
- Delete: A7DS1, A7E1, A7MP1, and A7XDS1.

Schematic 2,
- Delete: +5-volt circuit from A7 to J4.

CHANGE 4

Table 6-2,
- A6: Change HP and Mfr Part Nos. to 01615-66506.
- A6C8: Change to HP Part No. 0140-0199, CAPACITOR-FXD, MICA, 240pF, 5%, 300V, Mfr Code 28480, Mfr. Part No. 0140-0199.
- Delete A6XU51.

Schematic 10A,
- A6R2/A6C3 Junction: Add TO U14 PIN 1.
- U51 Pin 11: Add TO U14 PIN 1.
- A6C8: Change value to 240 pF.

Schematic 10B,
- U14A pin 1: Show signal from A6R2/A6C3 junction.

CHANGE 5

Table 6-2,
- A5: Change HP and Mfr Part Nos. to 01615-66515.
- Add A5R38, HP Part No. 0757-0280, RESISTOR 1K 1% .125W F TC=0±100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-1001-F.

Schematic 8B,
- U18C: Disconnect pin 9 and reconnect it to +5V through new resistor A5R38, 1000 ohms.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains schematics, component location drawings, and troubleshooting information for making repairs to the 1615A. The component location drawings are placed just ahead of the schematic(s) which show most of the parts on the assembly. Table 8-1 lists the drawings contained in this Section.

Table 8-1. 1615A Schematics

Circuitry	Schematic No.
Assembly A1	
Data Probe Inputs	4A
Qualifier Multiplexer	4B
Memory Address MIC and MAC	4C
Assembly A9	
Probe Thresholds	4D
Assembly A2	
Clocks	7A
Trigger and Delay	7B
Trigger and Clock	7C
Assembly A3	
16-bit Memory	6A
Glitch Trigger	6B
Assembly A4	
Data Acquisition	5A
P/O Glitch Detectors	5B
P/O Glitch Detectors	5C
Assembly A5	
Microprocessor and ROM	8A
Trigger Line/Keyboard Pulse/Expand Indicator/Display Control/Memory Dump	8B
Assembly A6	
Video Timing Logic	10A
Microprocessor RAM and Alpha-numeric Generator	10B
Timing and Video Logic	10C
Assembly A7	
Power Supply	2
Assembly A8	
Mother Board	1
Assembly A13	
Display Driver	3
Assembly A10	
Keyboard	9

8-3. TROUBLESHOOTING WITH STATUS CODES.

8-4. If a malfunction is detected during certain instrument self tests, the 1615A will halt the test and display a status code on screen. The status code indicates machine status at the time that the malfunction was detected. Proper interpretation of the status code offers a clue to the nature of the malfunction.

8-5. A typical display of a status code is TEST FAILED, STATUS = 271. The status code is an octal number. It contains the status of seven different 1615A functions. Each function is assigned a different binary weight. A binary 1 indicates that the associated status is true; binary 0 indicates that the status is false. The following instrument status statements are included in the status code:

XXX

0 - NOT USED — ALWAYS LOW
1 - NOT USED — ALWAYS HIGH
X - 8-BIT MEMORY IS VALID

X - 16-BIT MEMORY IS VALID
X - EXTERNAL CLOCK IS RUNNING
X - NO 8-BIT TRIGGER

X - NO 16-BIT TRIGGER
X - 8-BIT RUN COMPLETE
X - 16-BIT RUN COMPLETE

8-6. The following description shows interpretation of the status code for TEST FAILED, STATUS = 271.

271

0 - NOT USED — ALWAYS LOW
1 - NOT USED — ALWAYS HIGH
0 - (FALSE) 8-BIT MEMORY IS VALID

1 - (TRUE) 16-BIT MEMORY IS VALID
1 - (TRUE) EXTERNAL CLOCK IS RUNNING
1 - (TRUE) NO 8-BIT TRIGGER

0 - (FALSE) NO 16-BIT TRIGGER
0 - (FALSE) 8-BIT RUN COMPLETE
1 - (TRUE) 16-BIT RUN COMPLETE

8-7. Status code 271 indicates the following:

The 8-bit memory is not valid.
The 16-bit memory is valid.
The external clock is running.
8-bit trigger has not been found.
16-bit trigger has been found.
8-bit run has not been completed.
16-bit run has been completed.

8-8. TROUBLESHOOTING WITH SELF TEST OF DATA-ACQUISITION HARDWARE.

8-9. During the self test of the data-acquisition hardware, the microprocessor sets up 21 traces, each with a different format and trace specification. For each trace, the 1615A makes a run and then the microprocessor reads the status code and first line on screen. This information is compared with the status code and first line that should be obtained in each test. If an error is detected in either the status code or first word, the microprocessor stops the self test immediately and displays the status code on screen. The CRT also displays the data obtained during the run if the trace was completed.

8-10. All of the data-acquisition circuitry is checked by the data-acquisition hardware self test, except for the following:

a. Data probes.
b. Clock qualifiers.
c. Internal clock.
d. Asynchronous trigger duration.
e. Glitch detection and triggering.
f. Time delay.
g. External trigger.

8-11. Table 8-2 lists the 21 traces which make up the data-acquisition hardware self test. The traces are performed in the order shown in the table. If the 1615A fails self test, compare the TRACE SPECIFICATION and FORMAT SPECIFICATION contained within the 1615A with table 8-2 to determine which one of the 21 traces failed. All preceding traces will have passed, and the 1615A will not have checked any of the traces that followed.

NOTE

The following conditions are true in all of the traces:

QUALIFIERS XXXXXX
8-BIT CLOCK .... EXTERNAL
8-BIT TRIGGER DURATION ..... 100 NS
GLITCH TRIGGER .... none

8-12. In the data-acquisition hardware self test, the input counter/latches (A1U31 through A1U34, A4U17, and A4U31) are configured as counters. The self-test clock from the front panel is supplied to the counter/latches which count from 00 to FF (hex) continuously. All six counter/latches are synchronized and all are reset at the same time so that they always have the same count.

8-13. If the self test fails, the counter/latches will remain in the counter mode until a change is made to either the FORMAT SPECIFICATION or the TRACE SPECIFICATION.

8-14. To perform the self test of the data-acquisition hardware, proceed as follows:

a. Connect the clock input lead from the clock pod to the SELF TEST CLOCK terminal on the 1615A front panel.
b. Hold the B key down on the keyboard and switch LINE power off and on.
c. Release the B key.
d. If this self test fails:

(1). Look at FORMAT SPECIFICATION and TRACE SPECIFICATION to determine which trace failed.

(2). Determine why trace failed by looking at the normal first line and status listed in table 8-2 and comparing with display on 1615A.

Table 8-2. Self Test of Data-acquisition Hardware

Trace	Trace Specification/ Format Specification Setup	Normal Test Results
1	MODE 24 BIT START TRACE trigger XXXXXX DELAY 000000 TRACE ALL STATES	FIRST LINE: 000 0B0B0B STATUS = 363
2	MODE 24 BIT START TRACE trigger XXXX DELAY 000000 TRACE ALL STATES	The trigger specified never occurs. This test makes sure there is no trigger recognition. Because the input counter/latches are synchronized, no data is captured and displayed. STATUS = 374
3	MODE 24 BIT START TRACE trigger XXXX DELAY 000000 TRACE ALL STATES	SAME AS TRACE 2
4	MODE 24 BIT START TRACE trigger XXXX DELAY 000000 TRACE ALL STATES	SAME AS TRACE 2
5	MODE 24 BIT START TRACE trigger 555555 DELAY 000000 TRACE ALL STATES	FIRST LINE: 000 555555 STATUS = 363
6	MODE 24 BIT START TRACE trigger AAAAAA DELAY 000000 TRACE ALL STATES	FIRST LINE: 000 AAAAAA STATUS = 363

Table 8-2. Self Test of Data-acquisition Hardware (Cont'd)

Trace	Trace Specification/ Format Specification Setup	Normal Test Results
7	MODE 24 BIT START TRACE trigger AAAAAA DELAY 1048575 TRACE ALL STATES	This trace checks that the 16/24-bit delay counters continue delay for a full 1048575 clocks. The μP stops the run before 1048575 clocks to find no trigger accepted and no run complete. The 1615A should display no data. STATUS = 374
8	MODE 24 BIT START TRACE trigger AAAAAA DELAY 000255 TRACE ALL STATES	FIRST LINE: 000 A9A9A9 STATUS = 363
9	MODE 24 BIT END TRACE trigger AAAAAA DELAY 000255 TRACE ALL STATES	FIRST LINE: 132 2E2E2E STATUS = 363
10	MODE 24 BIT START TRACE trigger X5X5X5 DELAY 000000 TRACE TRIGGER EVENTS	FIRST LINE: 132 555555 STATUS = 363
11	MODE 24 BIT START TRACE trigger X0X0X0 DELAY 000005 TRACE TRIGGER EVENTS	FIRST LINE: 132 555555 STATUS = 363
12	MODE 8 BIT START TRACE trigger 54 DELAY 000000	FIRST LINE: 000 55
13	MODE 8 BIT START TRACE trigger AA DELAY 000000	FIRST LINE: 000 AB STATUS = 363
14	MODE 8 BIT START TRACE trigger AA DELAY 1048575	SAME AS TRACE 7, EXCEPT FOR 8-BIT DELAY COUNTERS.
15	MODE 8 BIT trigger AA DELAY 000255	FIRST LINE: 000 AA STATUS = 363
16	MODE 8 BIT END TRACE trigger AA DELAY 000255	FIRST LINE: 000 AB
17	MODE 16 & 8 BIT 8 TRIGGERS 16 16-BIT: START TRACE 8-BIT: START TRACE trigger AA DELAY 000255	FIRST 16-BIT LINE: 000 AAAA FIRST 8-BIT LINE: 000 AA STATUS = 363
18	MODE 16 & 8 BIT 8 ARMS 16 16-BIT: START TRACE trigger XXXX DELAY 000000 8 BIT: START TRACE trigger AA DELAY 000000	FIRST 16-BIT LINE: 000 ACAC FIRST 8-BIT LINE: 000 AB STATUS = 363
19	MODE 16 & 8 BIT 16 ARMS 8 16-BIT: START TRACE trigger AAAA DELAY 000000 8 BIT: START TRACE trigger XX DELAY 000000	FIRST 16-BIT LINE: 000 AAAA FIRST 8-BIT LINE: 000 AB STATUS = 363
20	MODE 16 & 8 BIT 16 TRIGGERS 8 16-BIT: START TRACE trigger AAAA DELAY 000000 8 BIT: START TRACE trigger XX DELAY 000000	FIRST 16-BIT LINE: 000 AAAA FIRST 8-BIT LINE: 000 AA STATUS = 363
21	MODE 16 & 8 BIT 8 ARMS 16 16-BIT: START TRACE trigger X5X5 OCCUR 000011 8 BIT: START TRACE trigger AA DELAY 000000	FIRST 16-BIT LINE: 000 5555 FIRST 8-BIT LINE: 000 AB STATUS = 363

8-15. TROUBLESHOOTING WITH SIGNATURE ANALYSIS.

8-16. GENERAL SIGNATURE ANALYSIS. Logic circuitry normally executes nonsequential program instructions. This places changing data patterns throughout the logic circuitry. The signature analysis test technique forces the microprocessor to continuously execute a limited test routine. This places repetative data patterns throughout the logic circuitry.

8-17. A signature analyzer is used to probe data points within the logic circuit. The signature analyzer displays a 4-digit alphanumeric code (signature) which characterizes the activity measured during the test period. This manual lists the signatures taken from a properly operating 1615A. If the listed signatures are the same as those obtained by your signature analyzer, the related logic circuit is operating properly. If other signatures are obtained, use normal troubleshooting techniques to locate the source of the malfunction.

8-18. SIGNATURE ANALYSIS TEST SETUPS. There are four separate test setups for troubleshooting the 1615A using signature analysis: DSA Setups A through D. Each test setup checks a different activity in the digital circuitry. The red letters printed on the schematics indicate the DSA setups to use when checking signatures on the associated IC pins. If A5U1 pin 5 has a D printed in red on the schematic, use DSA Setup D when checking the signature on that IC pin. Each of the four DSA setups are described in the following paragraphs.

8-19. DSA SETUP A. This setup is used to collect signatures from each of the eight lines in the data bus over that portion of the microprocessor address range where ROM 0 through ROM 5 are active.

8-20. The bidirectional data buffers (A5U12 and A5U24) are removed from A5 to isolate the microprocessor from the data bus. The DSA jumper on A5 is placed in the SA position during this test setup to apply the MOV A TO A instruction to the microprocessor. This causes the microprocessor to continuously perform a read and then increment its address. The signature analyzer is connected so that it turns on when ROM 0 is enabled and turns off when ROM 5 is disabled.

8-21. DSA SETUP B. This setup consists of seven separate DSA test setups: (B0 through B6). Each separate DSA setup is used to collect the signatures on the data bus that are supplied by only one of the five ROM's. DSA setup B0 takes the signatures from ROM 0, B1 takes signatures from ROM 1, etc.

8-22. The equipment setup for each of these tests is the same as for DSA Setup A, except that the signature analyzer start and stop lines are connected to the chip-select pin of the ROM to be analyzed: chip select of ROM 0 in DSA Setup B0, etc.

8-23. DSA SETUP C. This setup is used to collect signatures from each of the sixteen lines in the address bus over the entire microprocessor address range. This setup is also used to obtain signatures from the address decoding circuits that are enabled during microprocessor read cycles.

8-24. The equipment setup for these tests is the same as for DSA Setup A, except that the signature analyzer start and stop lines are connected to address bit 15 from the microprocessor. The signature analyzer starts when bit 15 goes high, and then stops when bit 15 goes high again. This establishes a measurement window that contains the entire microprocessor address range.

8-25. DSA SETUP D. This setup is used to collect signatures from each of the sixteen lines in the address bus over the entire microprocessor address range. This setup is also used to obtain signatures from the address decoding circuits that are enabled during microprocessor write cycles.

8-26. The bidirectional data buffers (A5U12 and A5U24) are removed from A5 to isolate the microprocessor from the data bus. For this test, the DSA jumper on A5 is left in the NM (normal) position. This applies the RESTART 7 instruction to the microprocessor, causing it to perform a write function and then decrement its address. The signature analyzer is clocked by the microprocessor write-not ($\overline{WR}$) line. The start and stop lines of the signature analyzer are connected to address bit 15 from the microprocessor. The signature analyzer is set to start when bit 15 goes high and stop when bit 15 goes high again. This allows the signature analyzer to capture a measurement window that contains the entire address range.

8-27. TROUBLESHOOTING AN INCOHERENT DISPLAY.

8-28. If the 1615A has an operating display, but the displayed information is random clutter, the cause of the 1615A malfunction can be detected by using the signature analysis procedures described for schematics 8A and 8B (the microprocessor assembly). To troubleshoot an incoherent display, proceed as follows:

a. Check the specified VH.

(1). If the VH is correct, proceed to step b.

(2). If the VH is not correct, check the power supplies, microprocessor clocks, and reset line. Make sure that the signature analyzer is connected and adjusted as specified in the procedure to be run. If all of these checks are correct, replace microprocessor A5U11.

b. Perform signature analysis procedures as described in DSA Setup A.

(1). If normal indications are obtained, check the buffers that were removed from A5. Then check RAM chips A6U15 through A6U17 and the control signals according to DSA Setup D. If all of the above are normal, check the other display driver IC's on A6.

(2). If abnormal indications are obtained, check DSA Setup C for A5U1 as described in step c.

c. Perform signature analysis procedures on A5U1 as described in DSA Setup C.

(1). If abnormal indications are obtained, replace A5U1 and recheck.

(2). If normal indications are obtained, check address buffers A5U10 and A5U23, and the address pins on microprocessor A5U11. If this does not locate the problem, then perform DSA Setup B to check the address lines on each ROM on A5. ROM 0 contains the self test that detects errors in the other ROM's. Check ROM 0 (DSA Setup B0) first. Before checking ROM 0, remove the other ROM's from A5 to avoid obtaining bad signatures due to interaction with an adjacent ROM.

8-29. TROUBLESHOOTING NO DISPLAY.

8-30. Use the following procedure to troubleshoot a 1615A which has no display:

a. Remove top and left side covers.

b. Apply power to 1615A and turn on LINE switch.

c. Check all power supply voltages to A13 (see schematic 3 and component locator on back of schematic 2).

d. Check high voltage circuit on A13. Horizontal deflection circuit and video amplifier require voltages from high voltage circuit.

e. Verify horizontal sync (HHSY), vertical sync (HVSY), and video (VIDEO) signals from A6 (schematics 10A through 10C).

f. Ground test point A13TP5. Observe fully unblanked horizontal and vertical raster (white screen) on 1615A CRT. If not, check waveform on A13TP4 to verify video amplifier operation.

g. Jumper A13TP5 to +5 volts. Display should be fully blanked. If not, check A13TP4 to verify video amplifier operation.

h. Check for deflection currents (spikes) at A13TP8 and A13TP9. A malfunctioning positioning circuit can place the display off screen. The deflection circuits can be isolated from the positioning circuits by removing A13R4 or A13R33; this will produce a slightly offset display.

i. If A13U6, A13Q1, or A13Q9 fail, check A13C2, A13C7, and A13C27. An open circuit or decrease in capacitance may permit a destructive increase in peak voltage across A13U6 or A13Q9.

j. Correction magnets on deflection coils are permanently attached and are not adjustable. Inspect them for damage if display distortion is observed.

8-31. SHOCK HAZARD MODIFICATION.

8-32. Instruments with serial numbers 1825A00626 and below may have a shock hazard on the line voltage terminals of the rear-panel power socket when the power cord is disconnected. A bleeder resistor installed across these terminals will eliminate the shock hazard. Remove the two screws holding the power socket to the rear panel and pull out the socket as far as possible. Solder a 4.7-megohm resistor (1/2-watt, carbon composition, HP Part No. 0687-4751) across the line voltage terminals. Then reinstall the socket.

8-33. ASSEMBLY A8 INTERCONNECTIONS. (See figure 8-1.)

8-34. Figure 8-1 shows signal paths on Mother Board A8 which interconnect assemblies A1 through A6. The PINS column lists each pin on connectors XA1 through XA6. The signal mnemonic is shown on each active trace. These mnemonics are the same as the mnemonics used on the schematics. The board assembly which is the source of each signal is identified by the letter S. The designation NC identifies pins which are not connected to the installed board assembly. Unless otherwise specified, all signals are TTL levels.

8-35. The following paragraph is an example showing the use of figure 8-1. Pin 7 of assemblies A1 and A2 are interconnected. The signal comes from A1, is the positive external trigger, and is an ECL signal. Pin 7 of assemblies A3 and A4 are connected together. A4 supplies the signal. It is sampled data bit 1 in the 8-bit instrument, a TTL signal.

8-36. MNEMONICS. (Refer to table 8-3.)

8-37. Signals in the 1615A have been assigned mnemonics that describe their active state and function. The first letter of each mnemonic indicates the active state of the signal. The remaining letters indicate signal function. When H is the first letter, it indicates that the function is active in the high state; L indicates that the function is active in the low state. For edge-controlled devices, P indicates that the function is active on the positive-going transition; N indicates that the function is active on the negative-going transition. Definitions of the mnemonics along with the numbers of the schematics where each signal originates are listed in alphanumeric order in table 8-3.

PINS	ASSEMBLIES ON MOTHER BOARD A8					
	A1	A2	A3	A4	A5	A6
1	O —5.2V	O	NC	O	O	O
2	O —5.2V	O	NC	O	O	O
3	O GND	O (ECL)	NC	O	NC	NC
4	O GND	O (ECL)	NC	O	NC	NC
5	O GND	NC (ECL)	NC	O	NC	NC
6	O +5V	NC	NC	O	NC	NC
7	S PETRG	O(ECL)	O H8SD1	S	S PDCLK	O
8	S NETRG	O(ECL)	O H8SD0	S	S NDCLK	O
9	S NECLK	O(ECL)	O H8SD3	S	O GND	NC
10	S PECLK	O(ECL)	O H8SD2	S	O GND	O
11	O N16SCLK	(ECL) S	O H8SD5	S	S PCLK6	O
12	O P16SCLK	(ECL) S	O H8SD4	S	NC	NC
13	O H16TRGL	S(ECL)	O H8SD7	S	NC	NC
14	O L16TRGL	S(ECL)	O H8SD6	S	S NCHCLK	O
15	O GND	O	O GND	O	O GND	NC
16	S H16QLY	O	O GND	O	O GND	NC
17	S H8QLY	O	O H8SG1	S	O HHB2	S
18	O GND	O	O H8SG0	S	O LHB2	S
19	O GND	O	O H8SG3	S	O LHB3	S
20	O L16MWRT	S	O H8SG2	S	S	O

Figure 8-1. Mother Board Assembly A8 Interconnections

PINS	A1	A2	A3	A4	A5	A6
	ASSEMBLIES ON MOTHER BOARD A8					
21	O P16CCLK	S	O H8SG5	S	S HTIME	O
22	O GND	NC	O H8SG4	S	NC	NC
23	S H16RCP	O	O H8SG7	S	NC	NC
24	NC GND	O	O H8SG6	S	S (SEE PIN 59) PCLK1	O
25	NC GND	O	O GND	O	O GND	NC
26	S H16VME	O	O GND	O	O GND	NC
27	O H16START	S	O LMACLD	NC	S	NC
28	NC GND	O	S PFILTERCLK	O	O LALPH	S
29	NC	NC	NC	NC	S LRAMA	O
30	NC	S LGLITCH SET	NC (ECL)	O	S HREAD	O
31	NC	S HGLITCH RESET	NC (ECL)	NC	S HWR	O
32	NC	S	NC L GLITCH RESET	O (ECL)	S HRAMW	O
33	NC	S N8SCLK	NC (ECL)	O	O GND	NC
34	NC	S P8SCLK	NC (ECL)	O	O GND	NC
35	NC	O GND	NC (ECL)	O	S HTLIN	O
36	NC	S L8TRGL	NC (ECL)	O	S HEXPI	O
37	NC L8ATG	O (ECL)	NC	S	NC	NC
38	NC H8ATG	O (ECL)	NC	S	NC	NC
39	O HD0ECL	NC (ECL)	NC	S	S HX1	O
40	NC GND	O (ECL)	NC	O	NC	NC

Figure 8-1. Mother Board Assembly A8 Interconnections (Cont'd)

PINS	ASSEMBLIES ON MOTHER BOARD A8					
	A1	A2	A3	A4	A5	A6
41	O LDACQ (ECL)	NC	NC	S	S HUPC	O
42	O LMRST	S	O	O	NC	NC
43	S L16/24STG	O (ECL)	NC	S	NC	NC
44	S VTH ADJ POD 1	NC	NC	O	S HSTD	O
45	S VTH RETURN POD 1	NC	NC	O	NC VIDEO	S
46	O L24BST	NC	NC	S	NC	NC
47	O L16TRC	S	O	NC	S HEXC	O
48	NC H16TFP	S	O	NC	NC HVSY	S
49	NC H16TDLY	S	O	NC	S LX1	O
50	NC	O L16AT8	S	S LDT	O	O
51	NC H8ECLK	S	O	NC	S HSTATE	NC
52	NC	O H8VME	S	NC	S LGL	O
53	NC	O H8TFP	S	NC	NC	NC
54	NC	O H8TDY	S	S HM2	O	NC
55	NC	O L8TRC	S	NC	O LALPH2	S
56	NC H8START	S	O	NC	NC HHSY	S
57	NC	O GND	O	NC	NC	NC
58	NC P8TCLK	S	O	S HM1	O	NC
59	NC	NC	NC	NC	S (SEE PIN 24) PCLK1	NC
60	O HW15	O	O	NC	S	O

Figure 8-1. Mother Board Assembly A8 Interconnections (Cont'd)

PINS	A1	A2	A3	A4	A5	A6
	ASSEMBLIES ON MOTHER BOARD A8					
61	NC	NC	NC	NC	NC —12V	○
62	NC	NC	NC	NC	○ +12V	NC
63	○ H16CTG	S	S HGTRG	○	NC	NC
64	NC	S H8CTG	○	NC	NC	NC
65	NC16/24BTOUT	S	S H8PAT	NC	NC	NC
66	NC HLDTG	S	○	NC	NC	NC
67	ADJ VTH ○ POD 1	○ GND	○	NC	○	NC
68	ADJ VTH ○ CLK	S N20MHZ	NC	NC	○	NC
69	ADJ VTH ○ PODS 2/3	○	NC	NC NMDCLK	S	NC
70	GND	○ GND	○	NC	○	NC
71	NC	S P8CCLK	○	NC	NC	NC
72	NC	S L8MWRT	○	NC	S HAB13	○
73	○ GND	○	○	NC	S HAB12	NC
74	NC	○ H8RCP	S	NC	S HAB11	NC
75	NC H8ATGT	S	○	NC	S HAB10	NC
76	NC	S HRST	○	○	S HAB9	○
77	NC	NC	NC	NC	S HAB8	○
78	NC	NC	NC	NC	S HAB7	○
79	NC	○ HAB6	NC	NC	S	○
80	NC HAB5	NC	○	NC	S	○

Figure 8-1. Mother Board Assembly A8 Interconnections (Cont'd)

PINS	A1	A2	A3	A4	A5	A6
	ASSEMBLIES ON MOTHER BOARD A8					
81	O HR14	O	O	NC	S	NC
82	O HAB4	NC	NC	NC	S	O
83	NC	O HAB3	NC	NC	S	O
84	NC HAB2	NC	O	NC	S	O
85	O HAB1	O	O	NC	S	O
86	NC	NC	NC	NC	NC	NC
87	O HDB7	O	O	NC	O	O
88	O HAB0	NC	O	NC	S	O
89	O HDB5	O	O	NC	O	O
90	O HDB6	O	O	NC	O	O
91	O HDB3	O	O	NC	O	O
92	O HDB4	O	O	NC	O	O
93	O HDB1	O	O	NC	O	O
94	O HDB2	O	O	NC	O	O
95	NC	S 16/24BTGOUT	NC	NC	NC	VIDEO RET O
96	O HDB0	O	O	O	O	O
97	O GND	O	O	O	O	O
98	O GND	O	O	O	O	O
99	O +5V	O	O	O	O	O
100	O +5V	O	O	O	O	O

Figure 8-1. Mother Board Assembly A8 Interconnections (Cont'd)

Table 8-3. 1615A Mnemonics

Mnemonic	Description	Signal Number	Origin
H16AR8	High 16-bit Arms 8-bit. Signal is true when using 16-bit arms 8-bit mode of triggering.	NA	Schematic 6B, A3U22 pin 6
H16DLY0	High 16-bit Delay = 0. Signal is true when 16-bit or 24-bit delay is 0.	NA	Schematic 7B, A2U22 pin 4
H16QLY	High 16-bit Clock Qualified. Signal is true when the qualification is met for the 16-bit menu selection. ORed with 8-bit qualifier during 24-bit mode of operation.	16	Schematic 4B, A1P4 pin 16
H16RCP	High 16-bit Run Complete. Signal is true when 16-bit memory is full in modes where selected trigger starts data acquisition.	27	Schematic 4C, A1P4 pin 23
H16START	High 16-bit Start Trigger. Signal is true when trigger delay starts data acquisition in 16-bit and 24-bit synchronous modes.	19	Schematic 7C, A2P1 pin 27
H16STE	High 16-bit Store Trigger Events. During trace events mode in 16-bit machine, signal true only when trigger is recognized. In all other modes, signal is always true.	22	Schematic 7B, A2P1 pin 63
H16TDLY	High 16-bit Trigger Delay. Signal is true after the end of the trigger plus selected delay period in 16-bit or 24-bit synchronous modes.	54	Schematic 7B, A2P1 pin 49
H16TFP	High 16-bit Trigger Flip-Flop. Signal is true after 16-bit or 24-bit trigger is recognized.	53	Schematic 7B, A2P1 pin 48
H16TR8	High 16-bit Triggers 8-bit. Signal is true when using the 16-bit triggers 8-bit mode, or 24-bit mode.	NA	Schematic 6B, A3U22 pin 3
H16TRGL (ECL)	High 16-bit Trigger Load, ECL. Enables 16-bit trigger memory to accept new data when true. Differential signal with L16TRGL(ECL).	7	Schematic 7A, A2P1 pin 13
H16VME	High 16-bit Valid Memory. Signal prevents trigger recognition until a full data memory is captured in end-trigger modes. True after 255 data words are captured.	28	Schematic 4C, A1P4 pin 26
H8ARM16	High 8-bit Arms 16-bit. Signal is true when using 8-bit arms 16-bit mode of operation.	NA	Schematic 7B, U2U22 pin 6
H8ATG (ECL)	High 8-bit Asynchronous Trigger, ECL. Signal true when asynchronous trigger specification is met. Differential with L8ATG(ECL).	34	Schematic 5A, A4P1 pin 38
H8ATGT	High 8-bit Asynchronous Trigger, TTL. Signal from 8-bit trigger circuitry.	51	Schematic 7C, A2P1 pin 75

Table 8-3. 1615A Mnemonics (Cont'd)

Mnemonic	Description	Signal Number	Origin
H8DLEXCK	High 8-bit Delay by External Clock. Signal is true when 8-bit machine is selected to delay by a number of external clocks, and false when 8-bit machine is using time delay.	0	Schematic 7C, A2U25 pin 6
H8DLY0	High 8-bit Delay = 0. Signal is true when 8-bit delay is 0.	NA	Schematic 6B, A3U22 pin 4
H8ECLK	High 8-bit External Clock. Signal is true when operating the 8-bit machine from an external clock.	46	Schematic 7A, A2P1 pin 51
H8QLY	High 8-bit Clock Qualified. Signal is true when the qualification is met for the 8-bit menu selection. ORed with 16-bit qualifier during 24-bit mode of operation.	17	Schematic 4B, A1P4 pin 17
H8RCP	High 8-bit Run Complete. Signal is true when 8-bit memory is full in modes where selected trigger starts data acquisition.	48	Schematic 6A, A3P1 pin 74
H8SD0 — H8SD7	High 8-bit Sampled Data. Eight-bit bus of sampled information to the 8-bit data memory.	30	Schematic 5A, A4P1 pins 7-14
H8SD0*— H8SD7*	High 8-bit memory of Sampled Data. Eight lines carrying sampled data from 8-bit memory.	44	Schematic 6A, A3P2 pins 11-18
H8SG0 — H8SG7	High 8-bit Sampled Glitch. Eight-bit bus of glitch information to the 8-bit glitch memory.	39	Schematic 5B, A4P1 pins 17-24
H8SG0*— H8SG7*	High 8-bit memory of Sampled Glitch. Eight lines carrying glitch information from 8-bit memory.	45	Schematic 6A, A3P2 pins 3-10
H8START	High 8-bit Start Trigger. Signal is true when trigger delay starts data acquisition in 8-bit machine.	47	Schematic 7C, A2P1 pin 56
H8STE	High 8-bit Store Trigger Events. During trace events mode in 8-bit machine, signal true only when trigger is recognized. In all other modes, signal is always true.	41	Schematic 7B, A2P1 pin 64
H8TDY	High 8-bit Trigger Delay. Signal is true after the selected trigger plus delay specification is met in the 8-bit machine.	55	Schematic 6B, A3P1 pin 54
H8TFP	High 8-bit Trigger Flip-Flop. Signal is true after 8-bit trigger is recognized.	58	Schematic 6B, A2P1 pin 53
H8TRG16	High 8-bit Triggers 16-bit. Signal is true when using 8-bit triggers 16-bit mode.	NA	Schematic 7B, A2U22 pin 3

Table 8-3. 1615A Mnemonics (Cont'd)

Mnemonic	Description	Signal Number	Origin
H8VME	High 8-bit Valid Memory. Signal prevents trigger recognition until a full memory is captured in end-trigger modes. True after 255 data words are captured.	49	Schematic 6A, A3P1 pin 52
HAB0 — HAB13	High Address Bus from microprocessor. Address lines from 8080A microprocessor on A5 board.	25	Schematic 8A, A5P1 pins 72-80, 82-85, 88
HD0ECL	High Data bit 0, ECL. Carries data for loading first 8 bits of 16-bit trigger memory.	5	Schematic 4A, A4P1 pin 39
HDB0 — HDB7	High Data Bus from microprocessor. Data to and from 8080A microprocessor A5U11.	26	Schematic 8A, A5P1 pins 87, 89-94, 96
HDLOC	High Delay by Trigger Occurrences. Signal is true when using delay by trigger occurrence mode.	NA	Schematic 7B, A2U22 pin 5
HDSP0	High Begin Display at Word 0. Signal is true when in timing diagram mode and data word 0 is to be displayed.	NA	Schematic 8B, A5U36 pin 19
HEXC	High Extra Cursor — not used. Always low.	NA	Schematic 10C, A5P1 pin 47
HEXPI	High Expand Indicator. Signal is high during display of the brightened (expandable area) segment of a timing diagram.	78	Schematic 8B, A5P1 pin 36
HEXTR	High External Trigger. Signal is true when using external trigger for 8-bit machine.	C	Schematic 7A, A2U3 pin 5
HGLITCHRESET (ECL)	High Glitch Reset, ECL. Not used in 1615A.	NA	Schematic 7A, A2P1 pin 31
HGTRGENA	High Glitch Trigger Enable. True during glitch trigger modes. Extends duration of asynchronous trigger to ensure proper glitch detection.	33	Schematic 6B, A3P1 pin 63
HHB2	High Horizontal Blanking 2. Signal is true during horizontal retrace.	74	Schematic 10A, A6P1 pin 17
HHSY	High Horizontal Sync. 20 kHz sync signal used to sync horizontal amplifier and low voltage power supply. Positive edge starts horizontal retrace.	1	Schematic 10A, A6P1 pin 56
HKDN	High Key Down. Signal is true when μP recognizes that a key is pressed.	73	Schematic 8B, A5U35 pin 8

Table 8-3. 1615A Mnemonics (Cont'd)

Mnemonic	Description	Signal Number	Origin
HLDTG	High Load Trigger. Signal is true when loading trigger memories prior to a run.	52	Schematic 7A, A2P1 pin 66
HM1	High Magnify No. 1. Always low. Part of preloaded count for expanded segment of timing diagram.	NA	Schematic 8B, A4P1 pin 58
HM2	High Magnify No. 2. Always low. Part of preloaded count for expanded segment of timing diagram.	NA	Schematic 8B, A4P1 pin 54
HPOS EDGE EXT TRG	High Positive Edge External Trigger. Signal is true when positive edge of external trigger is selected to turn on the 8-bit machine. Signal is false when negative edge selected.	NA	Schematic 7C, A2U25 pin 19
HR14	High Read 14. True when microprocessor commands a read other than ROM or RAM. Used in reads of 16-bit memory, 8-bit memory, or instrument status from assembly A2.	24	Schematic 8A, A5P1 pin 81
HRAMW	High RAM Write. Timing signal used when writing to display RAM. ANDed with HWR and LRAMA.	65	Schematic 8A, A5P1 pin 32
HREAD	High Read. This signal is true when microprocessor is reading.	68	Schematic 8A, A5P1 pin 30
HRST	High Reset 900 nsec. Pulse initializes the glitch detectors, and the 16-bit and 8-bit trigger and delay circuitry. The negative transition starts the run.	37	Schematic 7C, A2P1 pin 76
HSTATE	High State display. Not used.	NA	Schematic 8B, A5P1 pin 51
HSTD	High Start Timing Diagram. Signal is true when 1615A is displaying timing diagram information.	80	Schematic 8B, A5P1 pin 44
HTIME	High display Timing diagram. Signal is true when display of timing-diagram information is selected.	83	Schematic 8B, A5P1 pin 21
HTLIN	High Trigger Line. Signal is high only when displaying the location of the trigger word in timing diagram.	77	Schematic 8B, A5P1 pin 35
HTRACE	High Trace. Signal is true during a data acquisition cycle. Used by μP to stop run when STOP key is pressed or after run is complete.	R	Schematic 7C, A2U25 pin 15

Table 8-3. 1615A Mnemonics (Cont'd)

Mnemonic	Description	Signal Number	Origin
HTRACEE	High Trace Events. Signal is true when using the trace trigger events capability of the 24-bit state mode.	BB	Schematic 7C, A2U25 pin 5
HUPC	High microprocessor Cycle.	64	Schematic 8A, A5P1 pin 41
HVSY	High Vertical Sync. Signal used to sync vertical amplifier in display driver. Positive transition initiates vertical retrace.	2	Schematic 10C, A6P1 pin 48
HW15	High Write 15. Signal is true when microprocessor A5U11 is outputting information on data bus to locations other than ROM or RAM.	10	Schematic 8A, A5P1 pin 60
HWR	High Write. Signal is true when microprocessor is writing.	69	Schematic 8A, A5P1 pin 31
HX1	High magnify display X1. Signal is true during unexpanded displays of timing diagrams. Low when expanding by X10.	81	Schematic 8B, A5P1 pin 39
HX10	High Magnify Display X10. Signal is true during expanded displays of timing diagrams and false during unexpanded displays.	82	Schematic 8B, A5P1 pin 49
KSTB	Keyboard Strobe. Current pulse that strobes selected column of keys on keyboard.	73	Schematic 8B, A5Q2 Col.
L16/24STG (ECL)	Low 16/24-bit Synchronous Trigger, ECL. True when selected synchronous trigger is recognized.	9	Schematic 4A/5A, A1P4/A4P1 pin 43
L16AT8	Low 16-bit Arms or Triggers 8-bit. Signal is true when either 16ARMS8 or 16TRG8 mode of triggering is selected.	57	Schematic 6B, A3P1 pin 50
L16MWRT	Low 16-bit Memory Write. Signal is true when data-acquisition circuitry is writing data into 16-bit memory.	18	Schematic 7A, A2P1 pin 20
L16TRC	Low 16-bit Trace Point. Signal is true after trigger plus delay specification is met in 16-bit machine.	23	Schematic 7B, A2P1 pin 47
L16TRGL (ECL)	Low 16-bit Trigger Load, ECL. Enables the 16-bit trigger memory to accept new data when true. Differential signal with H16TRGL(ECL).	6	Schematic 7A, A2P1 pin 14
L24BST	Low 24-Bit State. Signal is true when 24-bit mode of data acquisition is selected. Configures 1615A for 24-bit synchronous operation.	15	Schematic 5A, A4P1 pin 46
L8ATG (ECL)	Low 8-bit Asynchronous Trigger, ECL. Signal true when asynchronous trigger specification is met. Differential with H8ATG(ECL).	35	Schematic 5A, A4P1 pin 37

Table 8-3. 1615A Mnemonics (Cont'd)

Mnemonic	Description	Signal Number	Origin
L8MWRT	Low 8-bit Memory Write. Signal is true when data-acquisition circuitry is writing data into 8-bit memory.	40	Schematic 7A, A2P1 pin 72
L8TRC	Low 8-bit Trace Point. Signal is true after trigger plus delay specification is met in 8-bit machine.	56	Schematic 7C, A2P1 pin 55
L8TRGL (ECL)	Low 8-bit Trigger Load, ECL. Enables both 8-bit trigger memories to accept new data when true.	29	Schematic 7A, A2P1 pin 36
LALPH	Low Alphanumeric display. Signal is true during displays of alphanumeric characters on 1615A CRT.	72	Schematic 10A, A6P1 pin 28
LALPH 2	Low Alphanumeric display 2. Signal is true during display of alphanumeric characters on 1615A CRT.	76	Schematic 10A, A6P1 pin 55
LDACQ (ECL) Also TTL on 5A	Low Data Acquisition, ECL. Parallel-enables all input data latches. True during data-acquisition modes. False during trigger memory load plus self-test.	8	Schematic 5A, A4P1 pin 41
LTD	Low Dual Threshold. Not used in 1615A. Normally high.	NA	Schematic 8B, A4P1 pin 50
LGL	Low Glitch. Signal is true when display of glitches is selected for timing diagrams, and high when glitch display is turned off.	84	Schematic 8B, A5P1 pin 52
LGLITCHRESET (ECL)	Low Glitch Reset, ECL. Positive edge resets glitch detection flip-flop at the start of each clock cycle.	38	Schematic 7A, A2P1 pin 32
LGLITCHSET (ECL)	Low Glitch Set, ECL. Preloads glitch detectors according to the logic levels at the start of each clock cycle.	36	Schematic 7A, A2P1 pin 30
LGLS	Low Glitch Set. Signal is true every tenth clock during expanded displays. It prevents multiple displays of a single glitch during expanded displays.	79	Schematic 8B, A5P1 pin 20
LHB2	Low Horizontal Blanking 2. Signal is true to blank display during horizontal retrace period.	71	Schematic 10A, A6P1 pin 18
LHB3	Low Horizontal Blanking 3. Signal is true during horizontal blanking to extend display blanking until arrival of next display clock.	75	Schematic 10A, A6P1 pin 19
LKR	Low Key Reset. Signal is true when μP is not reading keyboard. When true, this resets keyboard latches.	73	Schematic 8B A5U35 pin 3

Table 8-3. 1615A Mnemonics (Cont'd)

Mnemonic	Description	Signal Number	Origin
LMACLD	Low Memory Address Counter Load. Parallel-enables MAC in 8-bit memory.	42	Schematic 7B, A5P1 pin 27
LMRST	Low Master Reset. True before a data-acquisition run to reset memory index and address counters and input latches in 8-bit and 16-bit machines.	21	Schematic 7C, A2P1 pin 42
LPCKS	Low Positive Clock Slope. True when positive edge of external clock is selected to obtain data. False when negative edge is selected.	K	Schematic 7C, A2U25 pin 16
LRAMA	Low RAM Address. Signal is true when microprocessor is addressing locations in the display RAM.	70	Schematic 8A, A5P1 pin 29
LRST	Low Reset. 900-ns true pulse that resets 16-bit trigger circuitry prior to a data-acquisition run. Positive transition starts the run.	NA	Schematic 7C, U50 pin 3
N16SCLK	Negative-edge 16-bit Sample Clock. Not used in 1615A.	NA	Schematic 7A, A2P1 pin 11
N20MHZ	Negative-edge 20-MHz clock. Clock source for microprocessor board. Available whenever 1615A has operating power applied.	59	Schematic 7A, A2P1 pin 68
N8SCLK	Negative-edge 8-bit Sample Clock. Not used in 1615A.	NA	Schematic 7A, A2P1 pin 33
NCHCLK	Negative-edge Character Clock. Clock for character counters used during alphanumeric displays.	63	Schematic 8A, A5P1 pin 14
NDCLK	Negative-edge Display Clock. Clocks for the character generator during alphanumeric displays and the graticule generator during timing diagram displays.	61	Schematic 8A, A5P1 pin 8
NECLK (ECL)	Negative-edge External Clock, ECL. External clock signal from clock probe for use in some data-acquisition modes. Differential of PECLK.	12	Schematic 4B, A1P4 pin 9
NETRG (ECL)	Negative-edge External Trigger, ECL. Negative edge of signal used to trigger data acquisition in 8-bit circuitry in external trigger modes. Supplied from clock probe. Differential of PETRG.	14	Schematic 4B, A1P4 pin 8
NMDCLK	Negative-edge Memory Dump Clock. Signal available only when dumping 8-bit memory to generate timing diagrams.	60	Schematic 8B, A5P1 pin 69

Table 8-3. 1615A Mnemonics (Cont'd)

Mnemonic	Description	Signal Number	Origin
P16CCLK	Positive-edge 16-bit Counter Clock. Clock that increments index and address counters in the 16-bit memory.	20	Schematic 7A, A2P1 pin 21
P16SCLK (ECL)	Positive-edge 16-bit Sample Clock, ECL. Signal clocks 16-bit input latches during data acquisition. Also derived from μP when loading trigger memories.	4	Schematic 7A, A2P1 pin 12
P8CCLK	Positive-edge 8-bit Counter Clock. Clock that increments index and address counters in the 8-bit memory.	43	Schematic 7A, A2P1 pin 71
P8SCLK (ECL)	Positive-edge 8-bit Sample Clock, ECL. Clock for 8-bit machine that controls operation within glitch detector circuits.	32	Schematic 7A, A4P1 pin 34
P8TCLK	Positive-edge 8-bit Trigger Clock. Clock for trigger plus delay counter in 8-bit machine.	50	Schematic 7A, A2P1 pin 58
PCLK1	Phase 1 Clock. Signal that clocks character lines in alphanumeric displays.	66	Schematic 8A, A5P1 pin 24
PCLK6	Phase 6 Clock. Signal that clocks the alphanumeric/time selector in the display assembly A6.	67	Schematic 8A, A5P1 pin 11
PDCLK	Positive-edge Display Clock. Clock for retrace counter, dot counter, line counter, and the alphanumeric/time display selector.	62	Schematic 8A, A5P1 pin 7
PECLK (ECL)	Positive-edge External Clock, ECL. External clock signal from clock probe for use in some data-acquisition modes. Differential of NECLK.	11	Schematic 4B, A1P4 pin 10
PETRG (ECL)	Positive-edge External Trigger, ECL. Positive edge of signal used to trigger data-acquisition in 8-bit circuitry in external trigger modes. Supplied from clock probe. Differential of NETRG.	13	Schematic 4B, A1P4 pin 7
VIDEO	Video. Z-axis unblanking signal to display driver. Least positive voltage turns on CRT.	3	Schematic 10C, A6P1 pin 45

8-38. DISCUSSION OF 1615A BASIC BLOCK DIAGRAM. (See figure 8-2.)

8-39. The 1615A is a microprocessor-controlled, ROM-based instrument consisting of a control section, display section, and a data-acquisition section. All sections share a common data bus, address bus, and control lines.

8-40. CONTROL SECTION. The control section of the 1615A consists of the keyboard, microprocessor, RAM, and ROM. Operator entries into the 1615A are made via the keyboard. The microprocessor controls all I/O, RAM, and ROM read/write activity as well as address bus and data bus usage. The 1615A capabilities, operating sequences, and self tests are all contained in ROM.

8-41. DATA ACQUISITION. The data-acquisition function of the 1615A consists of a 16-bit data-acquisition function and an 8-bit data-acquisition function. Each function has its own probes and I/O control. The 16-bit data-acquisition function gathers synchronous state data on up to 16 probe input lines. The 8-bit data-acquisition function has all of the capabilities of the 16-bit data acquisition function, except that it obtains information on 8 input lines. The 8-bit data-acquisition function also has the capability of gathering asynchronous activity on its 8 probe lines, and of detecting glitches occurring on any of those same 8 lines.

NOTE

The 24-bit mode is obtained by operating both the 16-bit and 8-bit machines together. Triggering is done in the 16-bit triggers 8-bit mode.

8-42. DISPLAY SECTION. The display section consists of RAM, I/O, alphanumeric display logic, timing diagram display logic, and the CRT. The RAM is loaded with the information obtained by the data-acquisition circuitry. The alphanumeric display logic reads 15 lines of RAM and formats the information into the electrical activity required for each alphanumeric character. The timing diagram display logic reads the entire RAM and presents a trace of electrical activity with respect to time. The electrical activity from one of the two display sections is converted to analog drive signals and supplied to the three axes of the CRT.

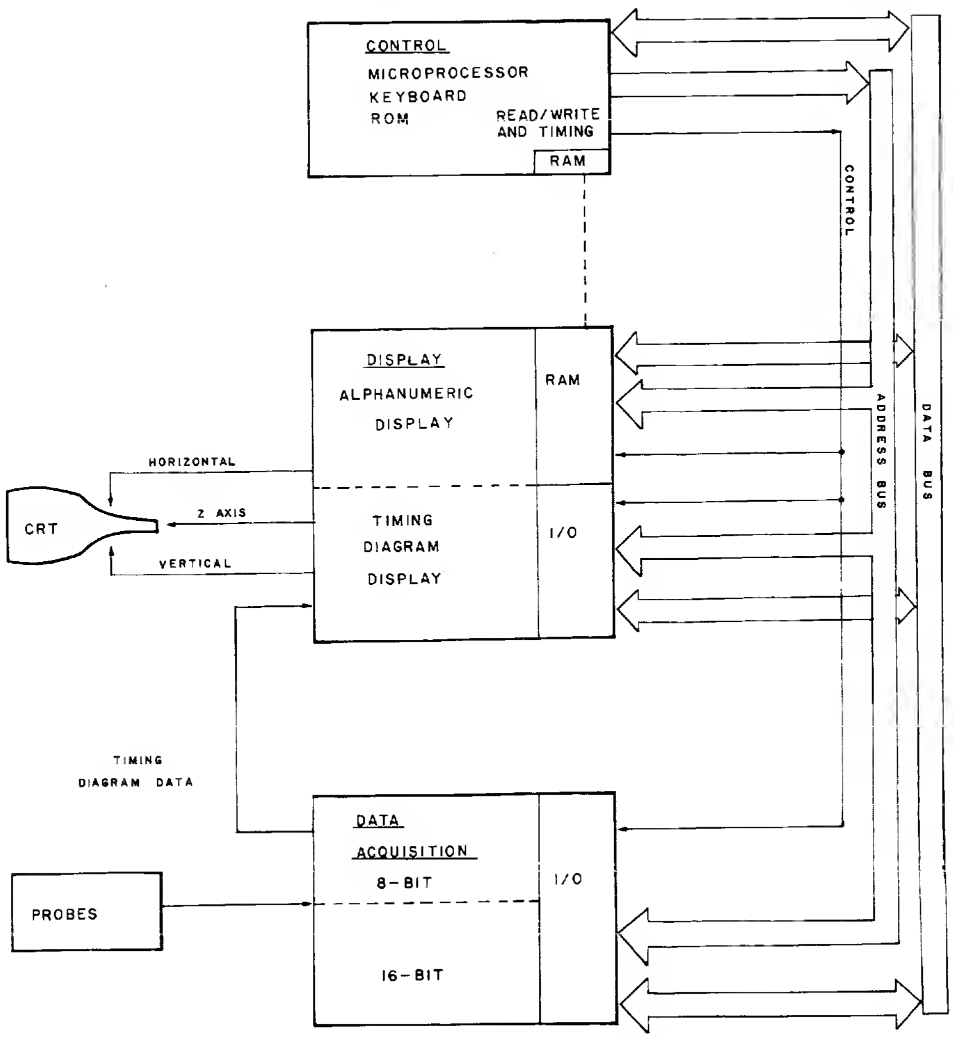


Figure 8-2. Model 1615A Basic Block Diagram

8-43. CONTROL SECTION BLOCK DIAGRAM. (See figure 8-3.)

8-44. The microprocessor controls all read/write and I/O activity on the address bus and data bus. The power on reset block holds the microprocessor in the reset state until its circuits can all be initialized after 1615A power up. The 20-MHz oscillator and divider supplies the proper clocks for microprocessor operation.

8-45. The program ROM's contain all of the 1615A test and operating routines. The RAM's provide active memory for the microprocessor and display functions. The keyboard provides operator interface to the 1615A instrument. .

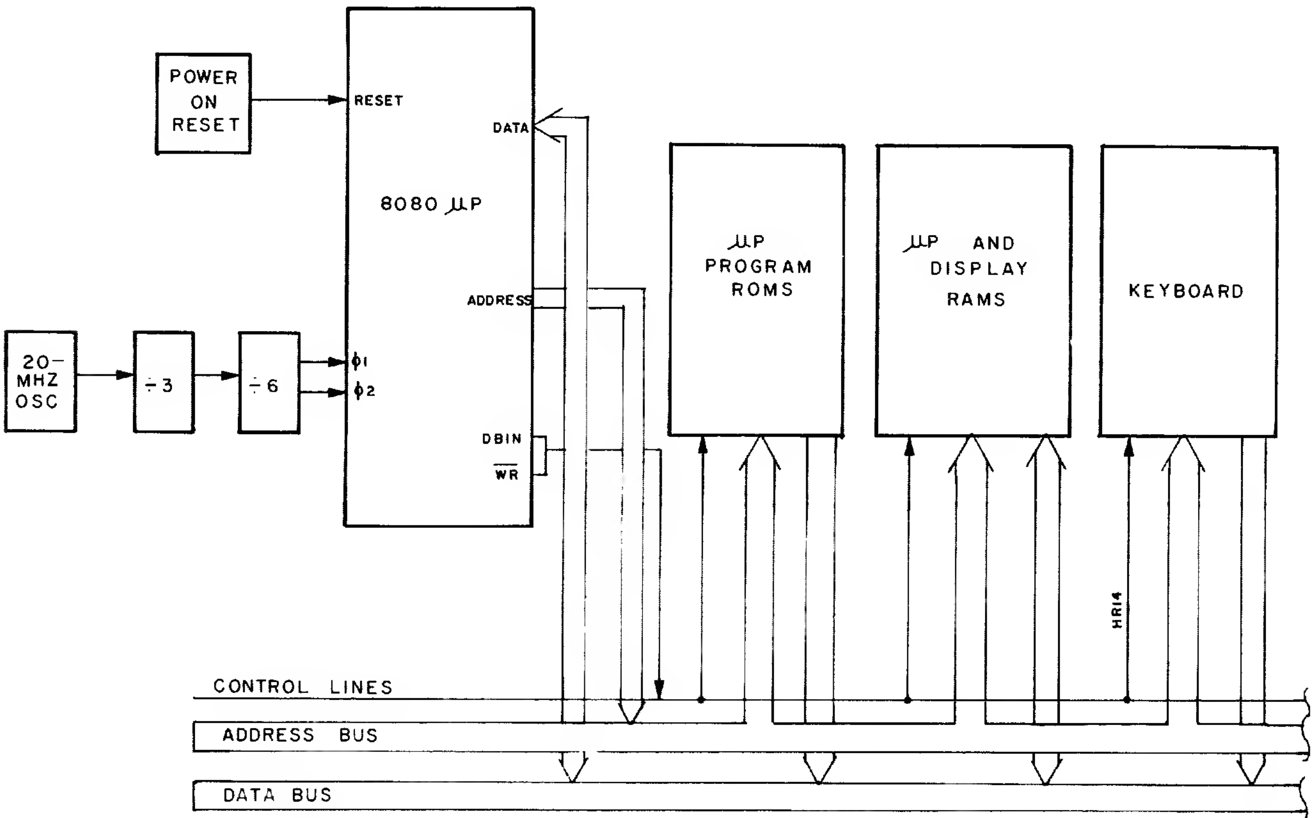


Figure 8-3. 1615A Control Section Block Diagram

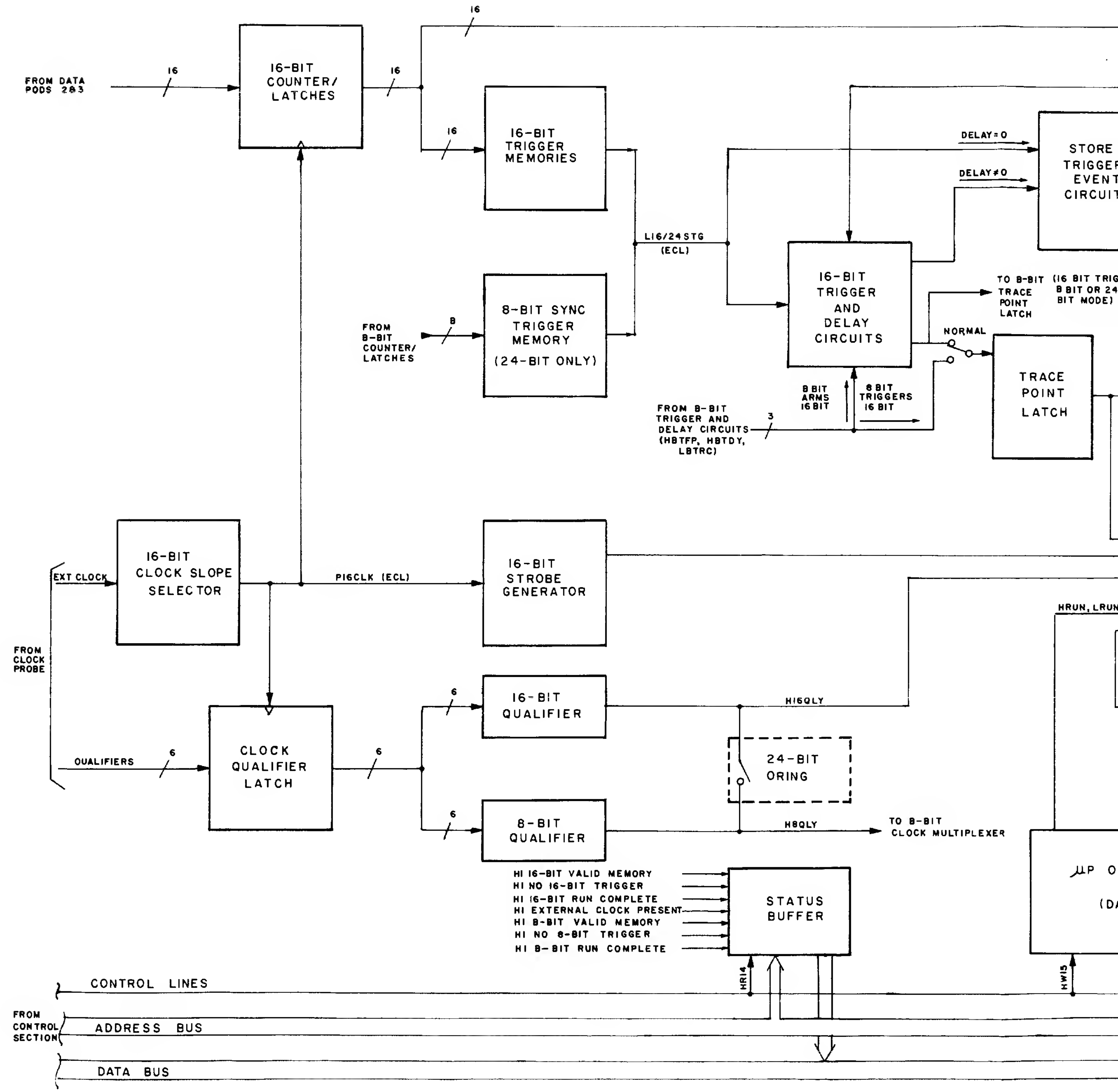
8-46. 16-BIT DATA-ACQUISITION SECTION BLOCK DIAGRAM DISCUSSION. (See figure 8-4.)

8-47. The 16-bit data-acquisition function collects state data that is synchronized with a clock. The state inputs are obtained through probe pods 2 and 3 and supplied to input latches. The clock is obtained by the clock probe and supplied to the clock slope selector. This block generates a pulse each time that it recognizes the occurrence of the selected edge on the clock line. The pulse latches the states of the lines from probe pods 2 and 3, and is also supplied to the 16-bit strobe generator and the clock qualifier latch. If all of the qualifier conditions are satisfied, H16QLY is delivered to the 16-bit clock multiplexer. At the same time, the 16-bit strobe generator delivers its strobe to the 16-bit clock multiplexer. If the qualifier conditions are satisfied, the strobe will be generated from the 16-bit clock multiplexer. If qualifier conditions are not satisfied, no strobe will be generated.

8-48. When the states on the 16 lines of the data probes are latched, they are supplied to both the 16-bit high-speed memory and to the trigger memory. If the states match the trigger conditions within the trigger memory, L16/24STG will be generated. This signal is supplied to the store trigger events circuit and to the trigger and delay block. These two blocks modify the trigger according to the mode of operation selected. In store trigger events mode, the store trigger events circuit only allows the states from the 16-bit counter/latches to be recorded in the high speed memory if they are a valid trigger word. In other modes of mixed triggering and delay, L16/24STG is supplied to the trace point latch only when all requirements of trigger interaction and delay are satisfied.

8-49. The trace point latch generates L16TRC when all trigger and delay requirements are met. When L16TRC is generated, the 16-bit memory index counter and the clock multiplexer are enabled. The clock multiplexer begins passing clocks from the strobe generator, and the memory index counter begins counting the clocks. These clocks also advance the memory address counter which sequentially addresses locations in the 16-bit high speed memory. When the memory index counter completes its count (a count equal to the number of memory locations available), the memory index counter triggers the run-complete condition which stops the clocks through the clock multiplexer. At this same time, the memory index counter supplies the address of the first word in memory to the read multiplexer.

8-50. The read multiplexer allows the microprocessor to address locations in memory and obtain memory contents for presenting a display on the CRT. The status buffer provides seven bits of status information to the data bus during and after completion run for data acquisition.



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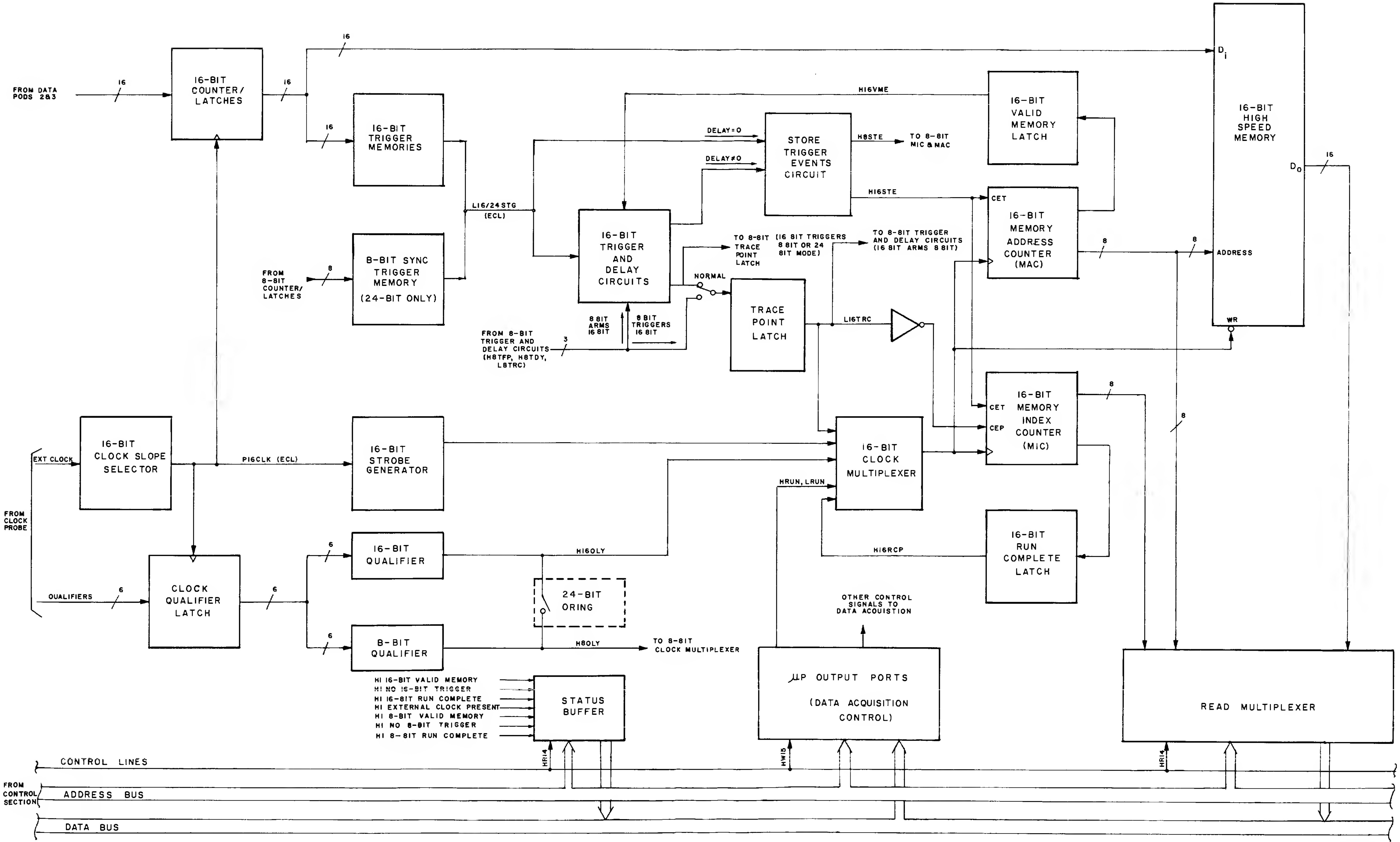


Figure 8-4. 16-bit Data-acquisition Block Diagram

8-51. 8-BIT DATA-ACQUISITION SECTION BLOCK DIAGRAM DISCUSSION. (See figure 8-5.)

8-52. The eight lines from pod 1 are supplied directly to the 8-bit counter/latch, the asynchronous trigger memory, and to the glitch detector. The 8-bit counter/latch operates the same as the counter/latch in the 16-bit circuitry, and is used only when the 8-bit and 16-bit machines are combined to capture 24-bit synchronous data. The asynchronous trigger memory generates its recognition state whenever it recognizes its trigger word on the eight lines from pod 1. The asynchronous trigger duration selector measures the time period of the recognition state from the asynchronous trigger memory. If the recognition state lasts for the entire time duration that the operator specified in the menu, the asynchronous trigger duration selector releases trigger recognition to the 1615A.

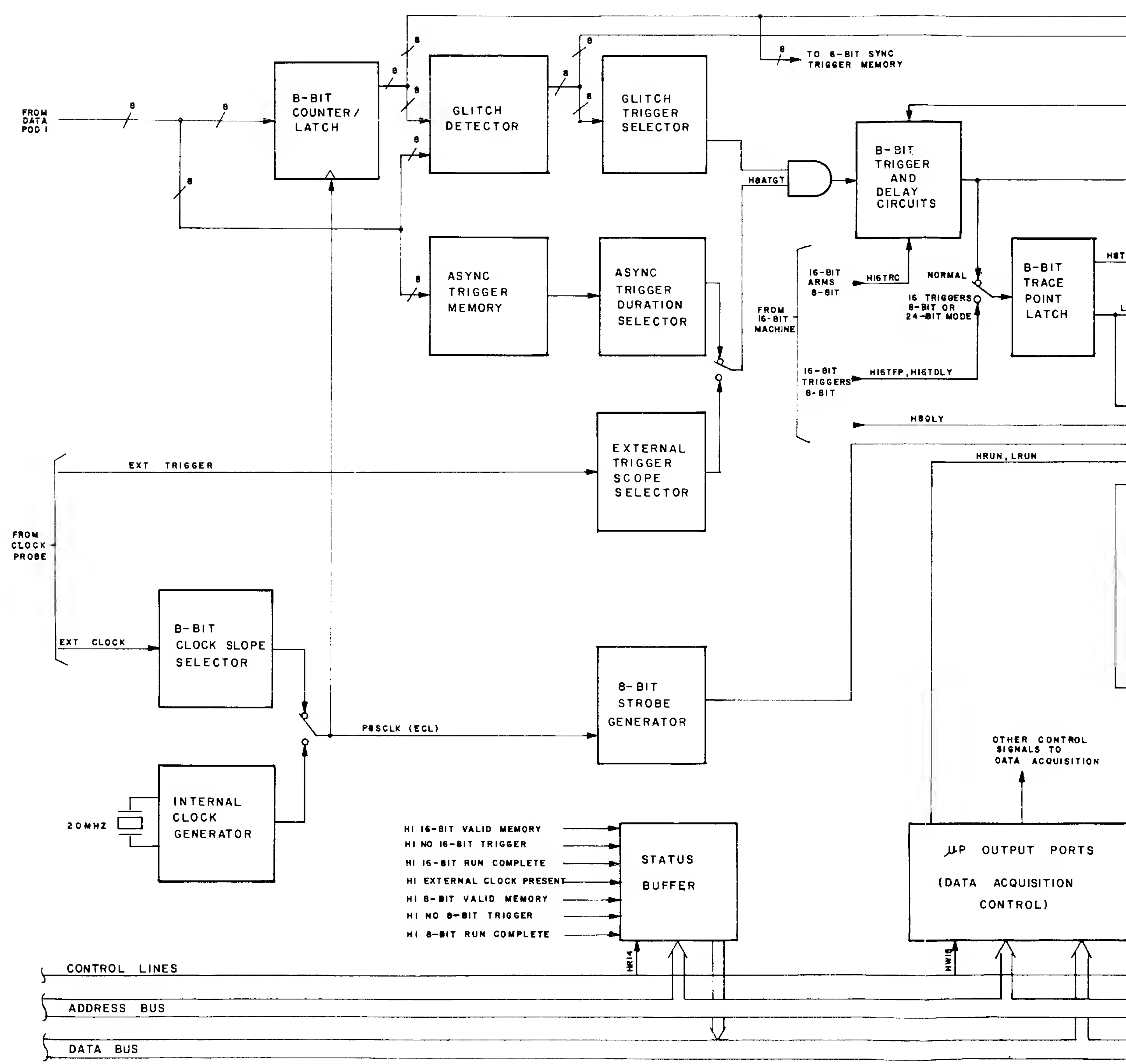
8-53. The glitch detector also receives the eight data lines from pod 1. If a glitch is detected on any line, a true state is supplied to the glitch memory and to the glitch trigger selector. If detection of a glitch was required as part of the trigger specification, then the gltich trigger selector supplies an enable at its output. If no glitch was specified as part of the trigger, then the glitch trigger selector always supplies the enable output.

8-54. The 8-bit trigger and delay circuits issue a trigger pulse according to the mode of trigger interaction selected in the 8-bit menu. H8VME is an enable level that is always present, except during modes where the trigger recognition ends the trace. In those modes, H8VME is only present after the 8-bit memory has accepted at least 256 valid inputs after the start of the run.

8-55. The 8-bit trace point latch enables the memory index counter to count qualified clocks so that the proper number of input bytes can be acquired into memory. When the memory index counter has counted the required number of input bytes (256 bytes in modes where the trigger starts the trace), it signals the 8-bit run complete latch which issues H8RCP to stop the run.

8-56. The clock for acquiring data into the 8-bit machine comes either from the external clock input (when the 8-bit machine is combined with the 16-bit machine) or from an internal clock generator. The internal clock generator provides several different clock rates to the 8-bit data-acquisition circuitry. The clock is delivered to the 8-bit clock multiplexer. When all qualification conditions are satisfied, the clock is coupled through the multiplexer to the 8-bit memory address counter, memory index counter, and to both the data and glitch memories. The memory address counter addresses sequential locations in memory for both the state and glitch information to be captured. The output from the 8-bit clock multiplexer also strobes the information into the memories.

8-57. The read multiplexer and status buffer provide the same operation for the 8-bit machine as is described for the 16-bit machine.



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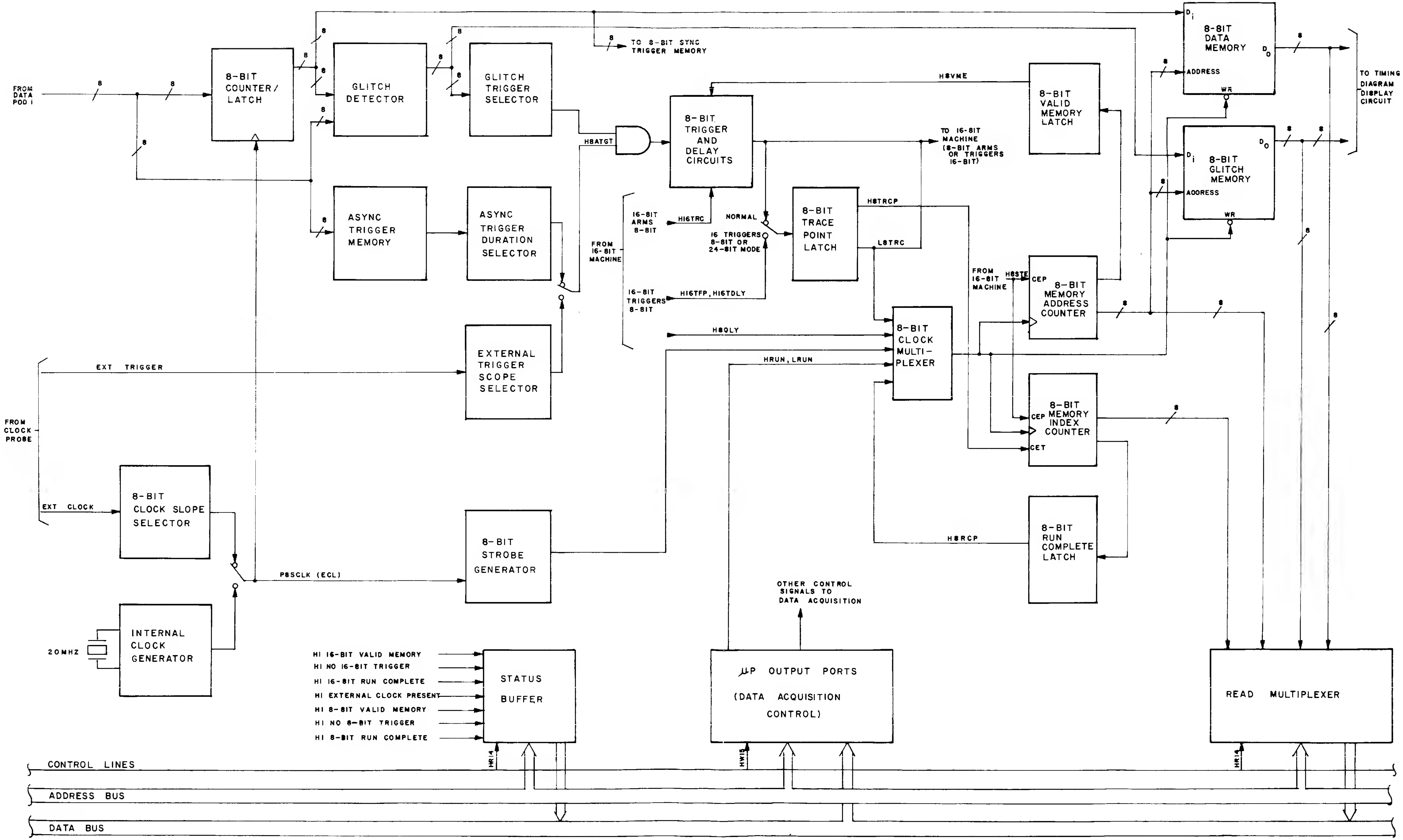


Figure 8-5. 8-bit Data-acquisition Block Diagram

8-58. DISPLAY SECTION BLOCK DIAGRAM DISCUSSION. (See figure 8-6.)

8-59. The display section consists of the alphanumeric character generator, the timing diagram generator, the display driver, and the alphanumeric/timing switch. The alphanumeric character generator reads portions of memory and presents the alpha and numeric characters on screen. The timing diagram generator reads the entire 8-bit memory and presents traces on screen that represent logical activity throughout the entire trace. The display driver accepts the formatted logic from the alphanumeric character generator and the timing diagram generator and drives the 1615A CRT.

8-60. ALPHANUMERIC/TIME SWITCH.

8-61. This block is controlled by menu selection and either activates the timing diagram generator or the alphanumeric character generator, depending upon the operating mode and position of the display on the CRT. The alphanumeric character generator is always active when presenting the heading on the CRT, regardless of whether the body of the display will be presented by the timing diagram generator or the alphanumeric character generator.

8-62. ALPHANUMERIC CHARACTER GENERATOR.

8-63. The alphanumeric character generator provides all of the video logic required to present all of the alphabetic and numeric characters on the CRT. Each character is made in a matrix of eight raster lines in heigth and five increments in width.

8-64. DOT AND RETRACE COUNTERS. These counters generate all of the horizontal steps across the CRT. The dot counter counts up for each progressive step across the CRT. The retrace counter counts back down to zero to accomplish CRT retrace.

8-65. LINE COUNTERS. These counters keep track of the vertical position on the CRT, and supply the format for each line. Some lines can be used for alphanumerics, some can also be used for timing diagrams, and some lines are always blanked.

8-66. CHARACTER COUNTER. The CRT is divided into 800 character spaces during alphanumeric displays (40 character spaces across each line by 20 lines). The character counter keeps track of which character space is being addressed on the CRT.

8-67. ADDRESS 2:1 SELECTOR. The address 2:1 selector obtains two addresses: one is the address of the character space being enhanced on the CRT, and the other is the microprocessor address bus. It supplies one of these two addresses to the display RAM.

8-68. DISPLAY RAM. Before a new display is placed on the CRT, the address 2:1 selector supplies the microprocessor address bus to the display RAM. At each microprocessor address, the data bus loads the appropriate character to be displayed on the CRT. During a display presentation, the address 2:1 selector supplies the address from the character selector to the display RAM. The addressed character stored in the RAM is displayed on the CRT.

8-69. MICROPROCESSOR LATCH. The microprocessor latch accepts the output from the display RAM. It supplies an output whenever the microprocessor reads information from the RAM.

8-70. CHARACTER CODE LATCH. This latch supplies the code for the character to be displayed on the CRT, along with codes for the character format, such as blinking and inverse video data.

8-71. CHARACTER GENERATOR ROM. This ROM translates the character code along with the format information from the line counters into the logic byte required to blank and unblank a particular raster scan in the 6X8 character matrix.

8-72. SHIFT REGISTER. The character generator ROM dumps the logic byte for the selected raster line into this shift register. The shift register supplies the logic byte bit-by-bit to the blinking and special effects gating.

8-73. BLANKING AND SPECIAL EFFECTS GATING. This circuit combines the raster line byte with logic for normal video, inverse video, blinking video, and blanking, as required for the display type selected in the menu. The output is supplied to the video gating where it is presented to the display driver for presentation on the CRT.

8-74. TIMING DIAGRAM GENERATOR SECTION.

8-75. FIRST WORD POSITION COUNTER. This counter always obtains the address of the first word in memory to be displayed on the timing diagram. This ensures that the portion of memory actually displayed on the timing diagram will be the proper segment for the operating mode selected (first 240 words in START TRACE mode, and last 240 words in END TRACE mode).

8-76. MEMORY ADDRESS COUNTER. This counter generates sequential addresses for the data memory and the glitch memory.

8-77. 8-BIT DATA MEMORY. This memory contains all of the data obtained from pod 1 during a trace. It supplies the binary data for all eight channels, byte-by-byte, to the 1 of 8 data selector.

8-78. 8-BIT GLITCH MEMORY. This memory contains all of the glitch information obtained in a trace for all eight timing diagram channels. It supplies the glitch information for all eight channels to the 1 of 8 glitch selector.

8-79. 1 OF 8 DATA AND GLITCH SELECTORS. This circuit chooses one of the eight data channels, along with the corresponding glitch channel, for display on the CRT. The selector is incremented from one channel to the next when the CRT display is incremented from one timing diagram slot to the next.

8-80. 2-BIT SHIFT REGISTER. This register holds both the bit that is to be displayed on the present point on the CRT, and the bit that was displayed on the last point on the CRT. This 2-bit information is used to determine whether or not the present bit is different from the last bit so that a transition can be included on the screen, if applicable.

8-81. TIMING DIAGRAM DISPLAY ROM. This ROM formats the display of data and glitch information for the timing diagram. In this ROM, data transitions, data locations, and glitch brighteners are computed. The outputs from this ROM provide all of the logic levels required for high and low displays, transitions, and glitch brighteners for both X1 and X10 display magnification.

8-82. X1/X10 SELECTOR. This unit selects either the X1 magnification signals or the X10 magnification signals for application to the video gating output.

8-83. CLOCK AND TIMING CONTROL. This circuit generates the operating rate within the circuitry that produces the timing diagram.

8-84. CHANNEL SELECTOR RAM. This RAM supplies an output that defines the location being addressed on the CRT. This information is used by the 1 of 8 data and glitch selectors to choose the channel it will supply to the display ROM. The channel select RAM also provides LO CHANNEL OFF to blank the display when the timing diagram slot on the CRT is turned off by operator selection.

8-85. EXPAND INDICATOR BLOCKS. The three blocks that make up this channel begin counting at the location where the expand indicator should begin, or where the trace should begin in X10 expanded display modes. This function counts a number of horizontal display increments across the CRT (that number equal to the width of the area displayed during X10 displays). HEXPI is true during this count.

8-86. TRIGGER MARKER. This function counts the number of horizontal locations on the CRT between the first sample and the sample which contains the trigger word. When this point is reached, the trigger marker function generates HTLIN which causes video gating to issue a trigger tic mark.

8-87. GRATICULE COUNTER. This counter provides a logic output that produces low level brightening at each horizontal location where a graticule line should be written on the CRT.

8-88. VIDEO GATING. This block produces an output which is the composite of the alpha, video, data, glitch, expand indicator, trigger tic marker, and graticule line enhancement. The level differs depending upon the signal mix at each sampled point across the CRT face.

8-89. DISPLAY DRIVER.

8-90. This section of the display circuitry drives the CRT. When alphanumeric characters are being presented, the horizontal and vertical sweep generators are controlled by the alphanumeric character generator. These two functions run at their own designed rates during timing diagram presentations. The Z-axis amplifier produces the unblanking levels required for all displays.

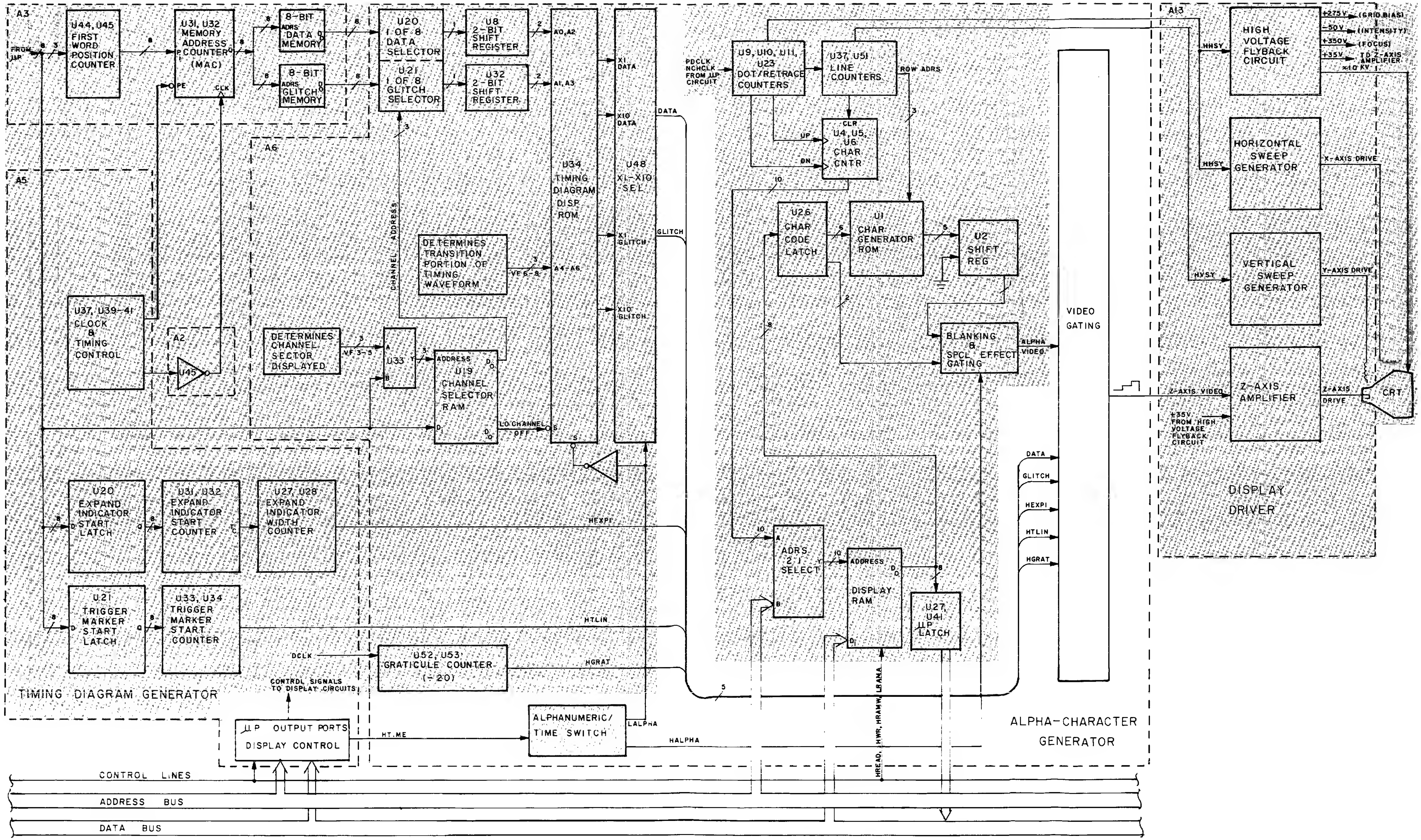


Figure 8-6.
Display Section Block Diagram

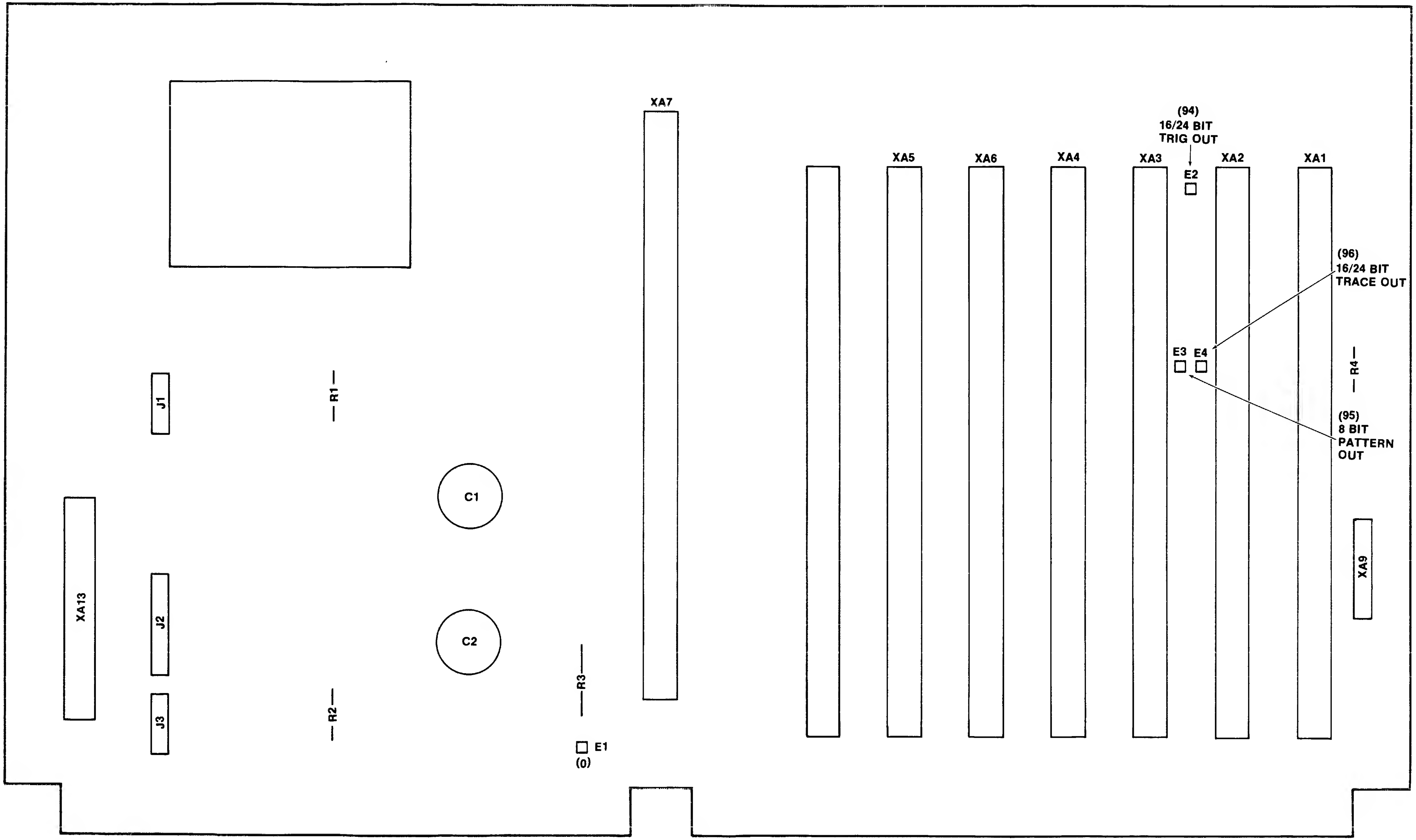


Figure 8-7. Mother Board Assembly A8, Parts Identification

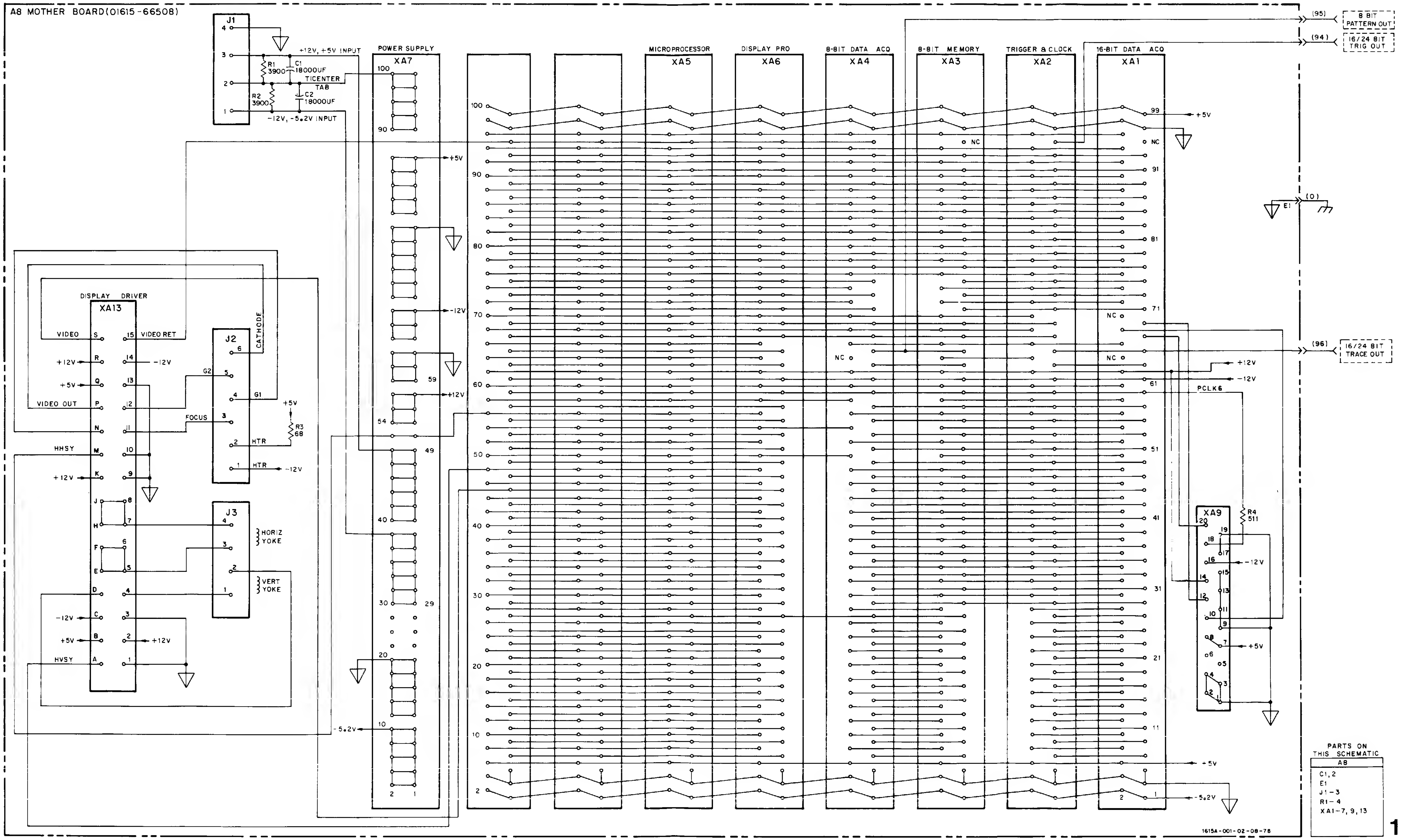
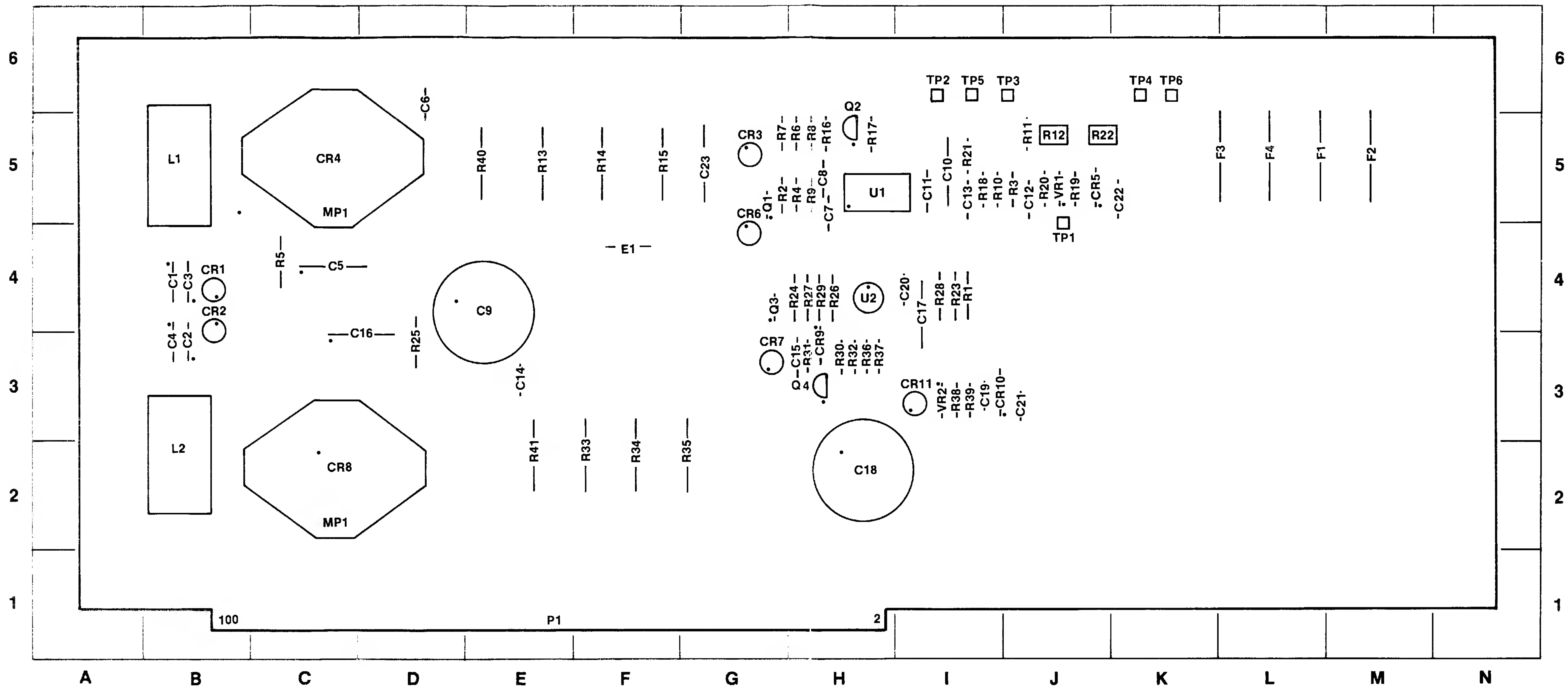
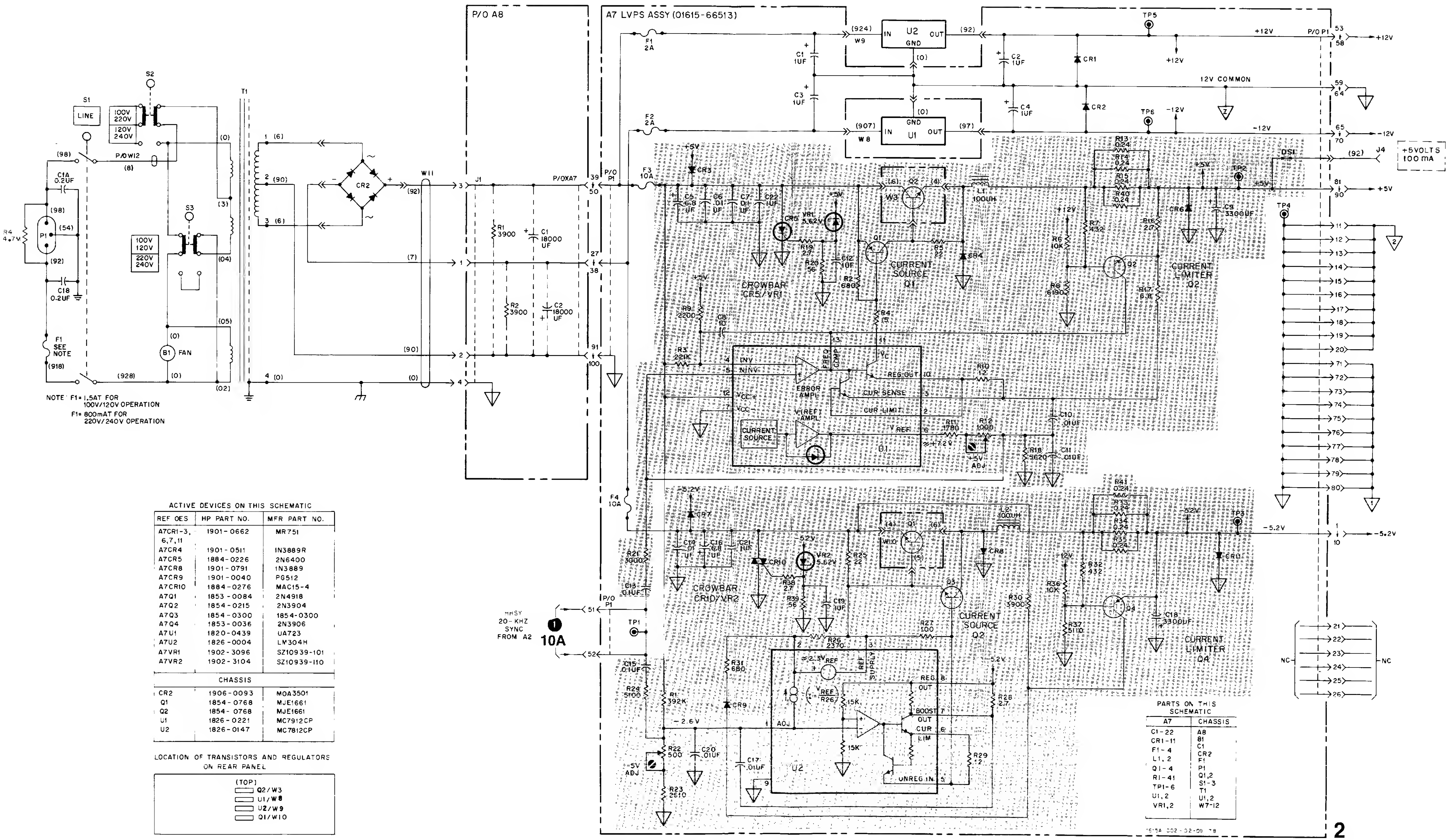


Figure 8-8.
Mother Board (A8) Schematic



REF DESIG	GRID LDC	REF DESIG	GRID LDC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LDC	REF DESIG	GRID LOC
C1	B-4	C16	D-3	CR7	G-3	P1	E-1	R10	I-5	R24	H-4	R3B	I-3
C2	B-3	C17	I-4	CRB	C-2	Q1	G-5	R11	J-5	R25	D-3	R39	I-3
C3	B-4	C1B	H-2	CR9	H-3	Q2	H-6	R12	J-5	R26	H-4	R40	E-5
C4	B-3	C19	I-3	CR10	I-3	Q3	G-4	R13	E-5	R27	H-4	R41	E-2
C5	C-4	C20	I-4	CR11	I-3	Q4	H-3	R14	F-5	R2B	I-4	TP1	J-4
C6	D-6	C21	J-3	E1	F-4	R1	I-4	R15	F-5	R29	H-4	TP2	I-6
C7	H-5	C22	K-5	F1	L-5	R2	G-5	R16	H-5	R30	H-3	TP3	J-6
CB	H-5	C23	G-5	F2	M-5	R3	J-5	R17	H-5	R31	H-3	TP4	K-6
C9	E-4	CR1	B-4	F3	L-5	R4	H-5	R1B	I-5	R32	H-3	TP5	I-6
C10	I-5	CR2	B-4	F4	L-5	R5	C-4	R19	J-5	R33	F-2	TP6	K-6
C11	I-5	CR3	G-5	L1	B-5	R6	H-5	R20	J-5	R34	F-2	U1	H-5
C12	J-5	CR4	C-5	L2	B-2	R7	G-5	R21	I-5	R35	G-2	U2	H-4
C13	I-5	CR5	J-5	MP1	C-2	R8	H-5	R22	J-5	R36	H-3	VR1	J-5
C14	E-3	CR6	G-5	MP1	C-5	R9	H-5	R23	I-4	R37	H-3	VR2	I-3
C15	H-3												

Figure 8-9. Low Voltage Power Supply Assembly A7, Parts Identification



ACTIVE DEVICES ON THIS SCHEMATIC

REF OES	HP PART NO.	MFR PART NO.
A7CR1-3, 6,7,11	1901-0662	MR751
A7CR4	1901-0511	1N3889R
A7CR5	1884-0226	2N6400
A7CR8	1901-0791	1N3889
A7CR9	1901-0040	PG512
A7CR10	1884-0276	MAC15-4
A7Q1	1853-0084	2N4918
A7Q2	1854-0215	2N3904
A7Q3	1854-0300	1854-0300
A7Q4	1853-0036	2N3906
A7U1	1820-0439	UA723
A7U2	1826-0004	LM304H
A7VR1	1902-3096	SZ10939-101
A7VR2	1902-3104	SZ10939-110
CHASSIS		
CR2	1906-0093	MOA3501
Q1	1854-0768	MJE1661
Q2	1854-0768	MJE1661
U1	1826-0221	MC7912CP
U2	1826-0147	MC7812CP

LOCATION OF TRANSISTORS AND REGULATORS ON REAR PANEL

(TOP)
Q2/W3
U1/W8
U2/W9
Q1/W10

PARTS ON THIS SCHEMATIC

A7	CHASSIS
C1-22	A8
CR1-11	81
F1-4	C1
L1, 2	CR2
Q1-4	F1
R1-41	P1
TP1-6	Q1,2
U1,2	S1-3
VR1,2	T1
	U1,2
	W7-12

1615A-002-02-09-78

2

Figure 8-10.
Low Voltage Power Supply (A7) Schematic

SERVICE SHEET 3

PRINCIPLES OF OPERATION

Display driver A13 generates signals to drive the display. The display is a magnetically-deflected, raster-scanned CRT. Display format is 20 lines of 40 characters each; each line consists of 9 horizontal scans of the CRT. Three signals from the A6 assembly, HVSY, HHSY, and VIDEO control the horizontal deflection, vertical deflection, and video amplifier circuits.

Horizontal Sync. HHSY (horizontal sync) controls the horizontal deflection circuit and the high-voltage supply. The HHSY signal is applied to U5 where, under normal operation, it is inverted, and used to drive U6. If the HHSY signal has an incorrect repetition rate or pulse width, U5 prevents the outputs of U6 from being on continuously, which would result in damage to U6. U6 provides a current pulse to the primary of T1. The secondary of T1 drives the horizontal deflection and high voltage circuits.

High-voltage Supply. The HV supply provides dc voltages for the CRT, bias voltage for the horizontal deflection circuit, and +35 volts for the video amplifier.

When Q9 is on, the current through L3 and the primary of T2 increases. When Q9 is turned off, energy stored in L3 and the primary of T2 rapidly charges C27. The result of the rapid charging is a large positive voltage across L3. This voltage is rectified by CR5 to provide the CRT accelerator grid bias. The positive voltage is also coupled to the secondaries of T2 where it is rectified.

Horizontal Deflection Circuit. The secondary of T1 also controls the horizontal deflection circuit. Just before Q1 is turned off, current is flowing in the deflection coil and the beam is at the right side of the CRT. When Q1 is turned off, the deflection coil current changes direction as C7 charges rapidly. After all the energy is transferred to C7, it then discharges through the coil, causing another change in direction of coil current. The rapid charge and discharge of C7 causes a rapid retrace of the beam. At the end of retrace, the voltage across the coil attempts to go negative and charge C7 again. When voltage across the coil reaches a few volts positive, CR1 turns on and becomes the current path for the coil. This voltage clamping by CR1 causes a constant rate of change in coil current. This accounts for the first half of horizontal scan. CR1 is turned on at a positive voltage, rather than zero, to compensate for resistive elements in the coil current path. This keeps the rate of current change from being greater at the beginning of the sweep than at the center or right side of the sweep.

When the beam reaches center screen, the deflection coil current is zero. At this time, Q1 is turned on and the current flow changes direction. This deflects the CRT beam toward the right side of the screen until Q1 turns off. When Q1 turns off, retrace begins.

Compensation for the deflection rate at the sides of the CRT is accomplished using C8. During the first half of the sweep the charge on C8 increases slightly. At center screen, when Q1 is turned on, C8 is slowly discharged, until the beam reaches the end of the sweep. This reduces voltage across the deflection coil at the beginning and end of the sweep, reducing the rate of current change in the coil.

Size of the horizontal scan is controlled by R6. R6 controls the voltage available to the deflection circuit by decreasing the coil current rate of change. Since the period of the sync signal does not vary, the scan will be shorter if the deflection rate is decreased.

Horizontal position is accomplished by injecting a constant current into the deflection coil. R14 determines the current. U1 compares voltage drops across C12 and R4, and drives Q2 and Q3 until the voltage drops are equal. This establishes a constant current through R4.

Vertical Deflection Circuit. This circuit generates the vertical sweep and controls height, linearity, and position of the sweep. Vertical sync (HVSY) from A6 controls a ramp generator, which in turn controls current through the deflection coil. When HVSY goes high, Q4 is turned on; this discharges C14 and C15 through R20. HVSY remains high for 0.5 millisecond (until capacitor charge returns to a few millivolts). When HVSY goes low, Q4 is turned off and C14 and C15 charge at a rate determined by R18 and R19. R18 controls amplitude of the vertical sweep. Since the period of HYSY is constant, R18 can be used to control the distance the beam is deflected within that period.

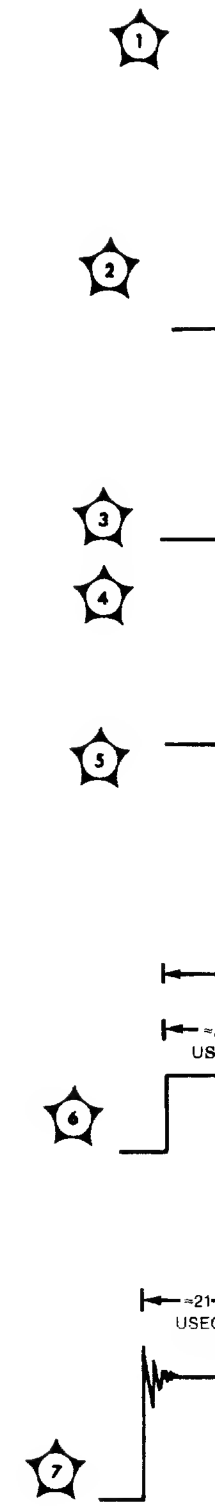
The voltage ramp developed at the junction of R20 and C14 is applied to U4. Part of the output of U4 is fed back to C14 and C15 to correct the voltage input of U4 which compensates the ramp generator. R23 controls the amount of feedback, which in turn controls the shape of the sweep generated. The ramp at the output of U4 drives current amplifier U3/Q5/Q6 which maintains a current through the emitter of Q6 that is proportional to the ramp voltage. U3 compares the ramp voltage to voltage across R32. U3 drives Q5 until the inputs to U3 are equal.

At the beginning of the sweep a very small current is flowing through Q6 and a large current is flowing from the +5-volt supply through deflection coil L1. This corresponds with the beam being at the top of the display. As the Q6 current increases, more current from the +5-volt supply flows through Q6 and less through the deflection coil. Coil current decreases and Q6 current increases until the beam reaches center screen. At that time, coil current has reached zero and begins to flow in the opposite direction as Q6 current starts to draw current from the coil and the +5-volt supply. When the beam reaches the bottom of the screen, coil current is about the same as it was at the top of the screen but is flowing in the opposite direction.

At the end of the sweep, Q6 is turned off abruptly, and the current through R32 is reduced to zero. This sudden change in coil current results in a positive voltage pulse at the collector of Q6. This charges C19, using energy stored in the deflection coil. This causes the beam to return to center screen as C19 reaches its peak voltage. C19 then discharges through R62 and the deflection coil. Discharge current and the current through L2 change the coil current direction and return the beam to the top of the CRT. At this time, Q6 starts conducting again and the sweep starts over.

Compensation for deflection rate at the top and bottom of the CRT is accomplished by C20 in a manner similar to that used in the horizontal deflection circuit. Position control is maintained by injecting a constant current into the deflection circuit through R33.

Video. This circuit amplifies the video signal to drive the CRT cathode. Gain control R61 is provided for contrast adjustment of the display.



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R4.

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20. HVSY
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R18 can be
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The voltage ramp developed at the junction of R20 and C14 is applied to U4. Part of the output of U4 is fed back to C14 and C15 to correct the voltage input of U4 which compensates the ramp generator. R23 controls the amount of feedback, which in turn controls the shape of the sweep generated. The ramp at the output of U4 drives current amplifier U3/Q5/Q6 which maintains a current through the emitter of Q6 that is proportional to the ramp voltage. U3 compares the ramp voltage to voltage across R32. U3 drives Q5 until the inputs to U3 are equal.

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Compensation for deflection rate at the top and bottom of the CRT is accomplished by C20 in a manner similar to that used in the horizontal deflection circuit. Position control is maintained by injecting a constant current into the deflection circuit through R33.

Video. This circuit amplifies the video signal to drive the CRT cathode. Gain control R61 is provided for contrast adjustment of the display.

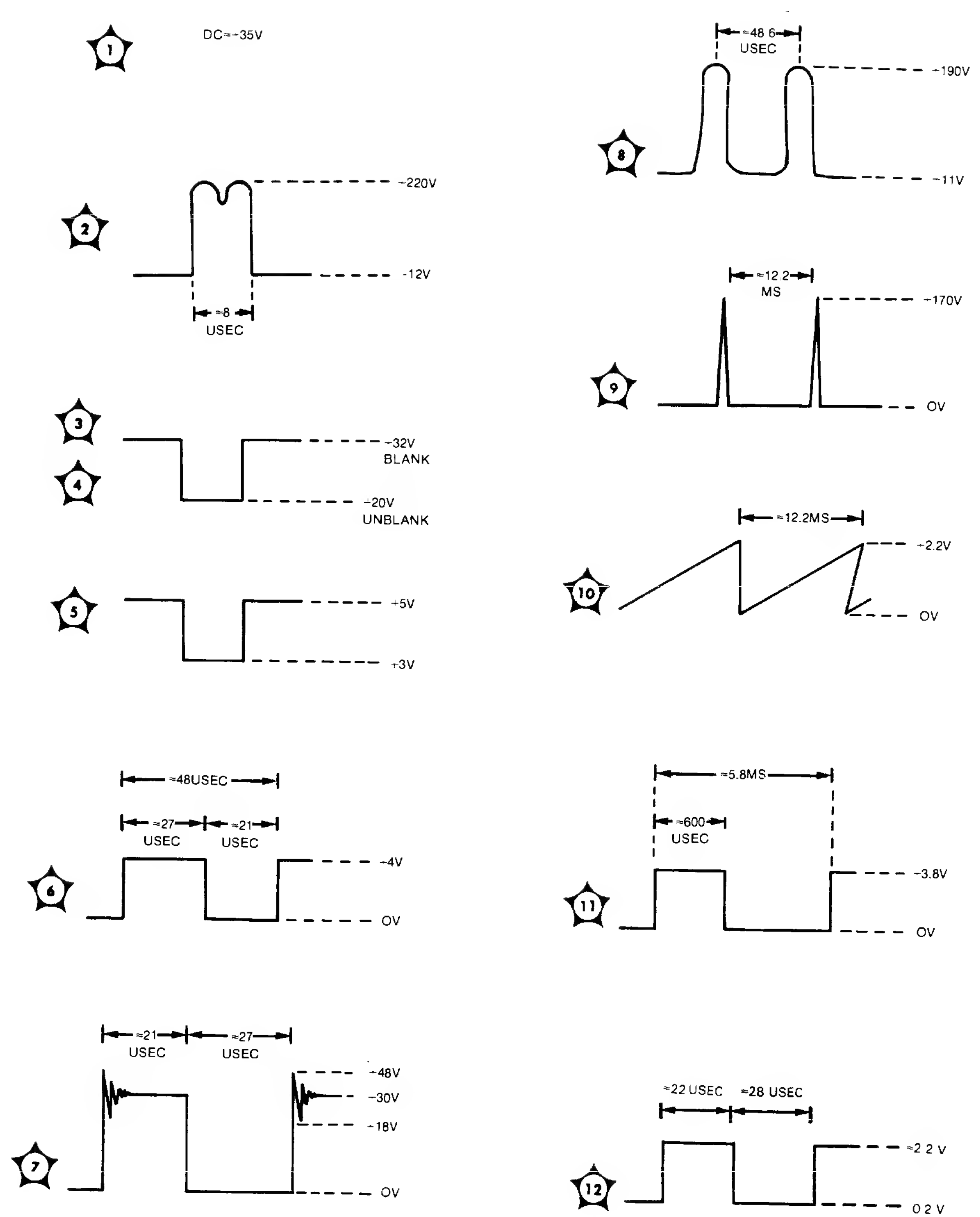


Figure 8-11. Model 1615A Display Waveforms

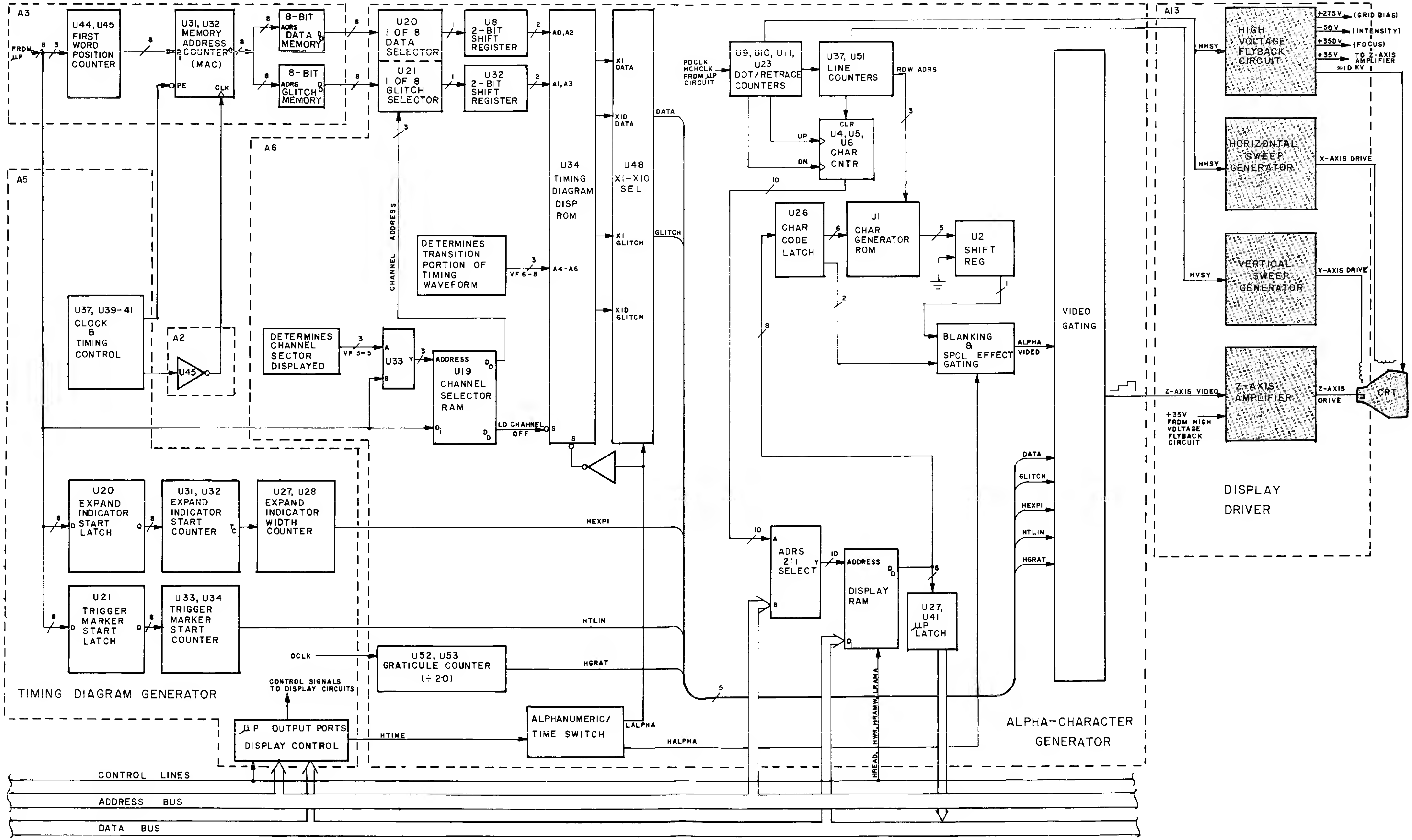
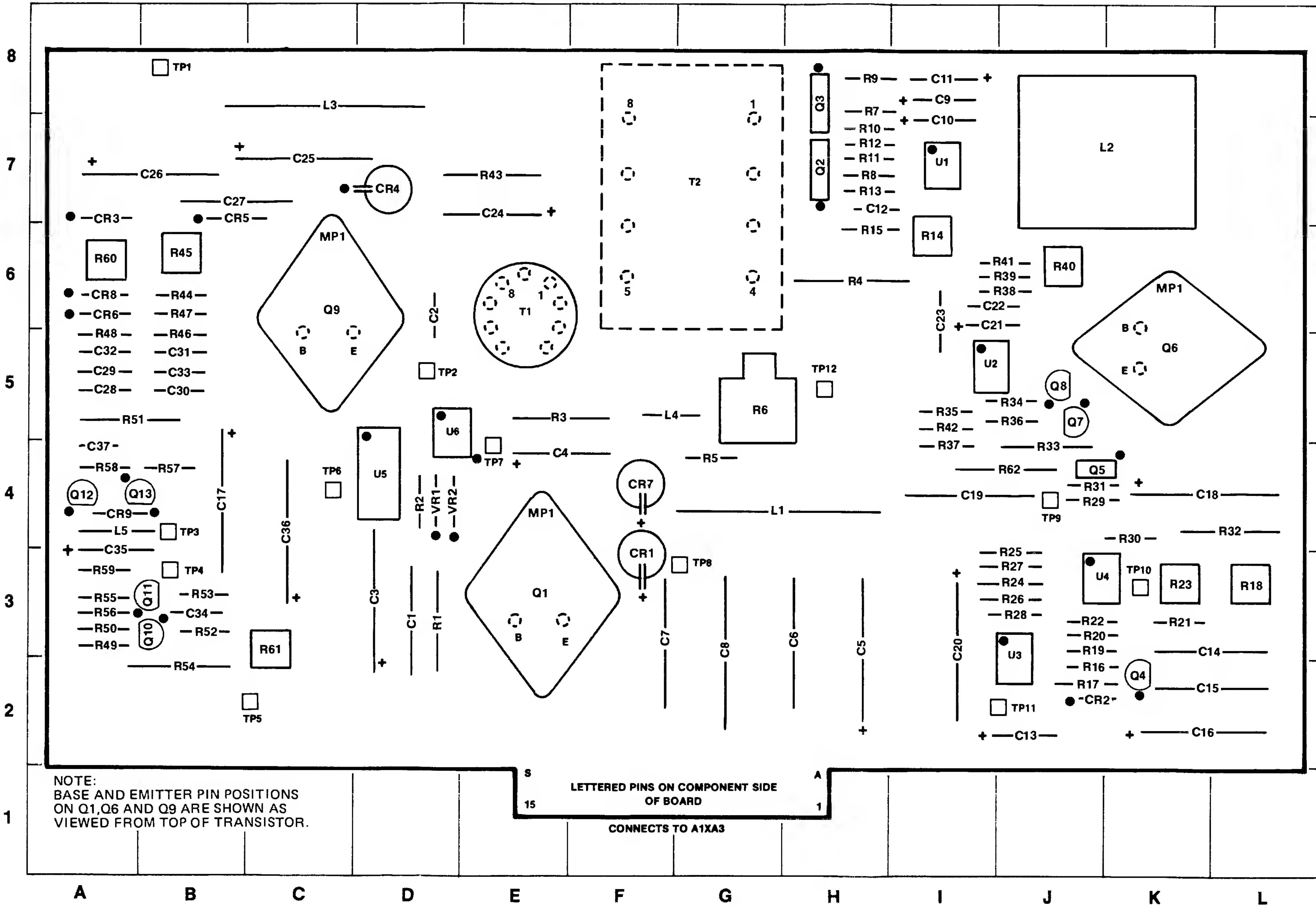


Figure 8-12.
Block Diagram of 1615A Display Section for Schematic 3



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-3	MP1	C-6	R36	J-5
C2	D-6	MP1	E-4	R37	I-4
C3	D-3	MP1	K-6	R38	J-6
C4	E-4	Q1	E-3	R39	J-6
C5	H-3	Q2	H-7	R40	J-6
C6	H-3	Q3	H-B	R41	J-6
C7	F-3	Q4	K-2	R42	I-5
CB	G-3	Q5	J-4	R43	E-7
C9	I-B	Q6	K-5	R44	B-6
C10	I-7	Q7	J-5	R45	B-6
C11	I-8	Q8	J-5	R46	B-5
C12	H-7	Q9	C-6	R47	B-6
C13	J-2	Q10	B-3	R48	A-5
C14	K-3	Q11	B-3	R49	A-3
C15	K-2	Q12	A-4	R50	A-3
C16	B-4	Q13	B-4	R51	A-5
C17	K-4	R1	D-3	R52	B-3
C1B	K-4	R2	D-4	R53	B-3
C19	I-4	R3	E-5	R54	B-2
C20	I-3	R4	H-6	R55	A-3
C21	I-6	R5	G-4	R56	A-3
C22	I-6	R6	G-5	R57	B-4
C23	I-6	R7	H-8	R5B	A-4
C24	E-7	RB	H-7	R59	A-3
C25	C-7	R9	H-B	R60	A-6
C26	B-7	R10	H-7	R61	C-3
C27	B-7	R11	H-7	R62	J-4
C2B	A-5	R12	H-7	T1	E-6
C29	A-5	R13	H-7	T2	G-7
C30	B-5	R14	I-6	TP1	B-8
C31	B-5	R15	H-6	TP2	D-5
C32	A-5	R16	J-2	TP3	B-4
C33	B-5	R17	J-2	TP4	B-3
C34	B-3	R1B	L-3	TP5	C-2
C35	A-3	R19	J-3	TP6	C-4
C36	C-4	R20	J-3	TP7	E-4
C37	A-4	R21	K-3	TP8	G-3
CR1	F-3	R22	J-3	TP9	J-4
CR2	J-2	R23	K-3	TP10	K-3
CR3	A-7	R24	J-3	TP11	J-2
CR4	D-7	R25	J-3	TP12	H-5
CR5	B-7	R26	J-3	U1	I-7
CR6	A-6	R27	J-3	U2	I-5
CR7	F-4	R28	J-3	U3	J-3
CRB	A-6	R29	J-4	U4	J-3
CR9	A-4	R30	K-4	U5	D-4
L1	G-4	R31	J-4	U6	D-5
L2	K-7	R32	L-4	VR1	D-4
L3	C-B	R33	J-4	VR2	D-4
L4	F-5	R34	J-5		
L5	A-4	R35	I-5		

Figure 8-13. Display Driver Assembly A13, Parts Identification

SERVICE SHEET 2

PRINCIPLES OF OPERATION

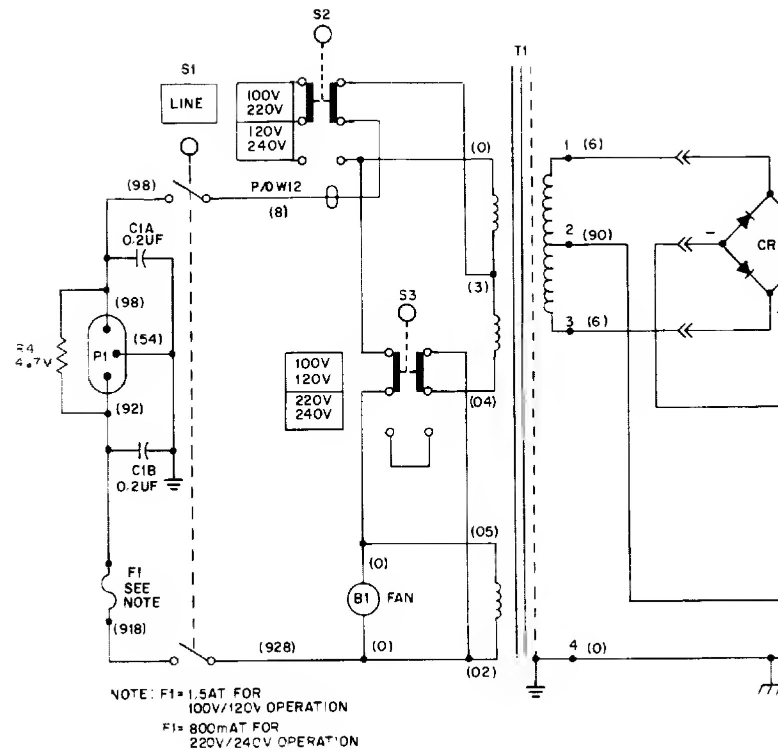
±12-volt Power Supplies. The +12-volt and -12-volt power supplies are regulated to within 5% by U1 and U2.

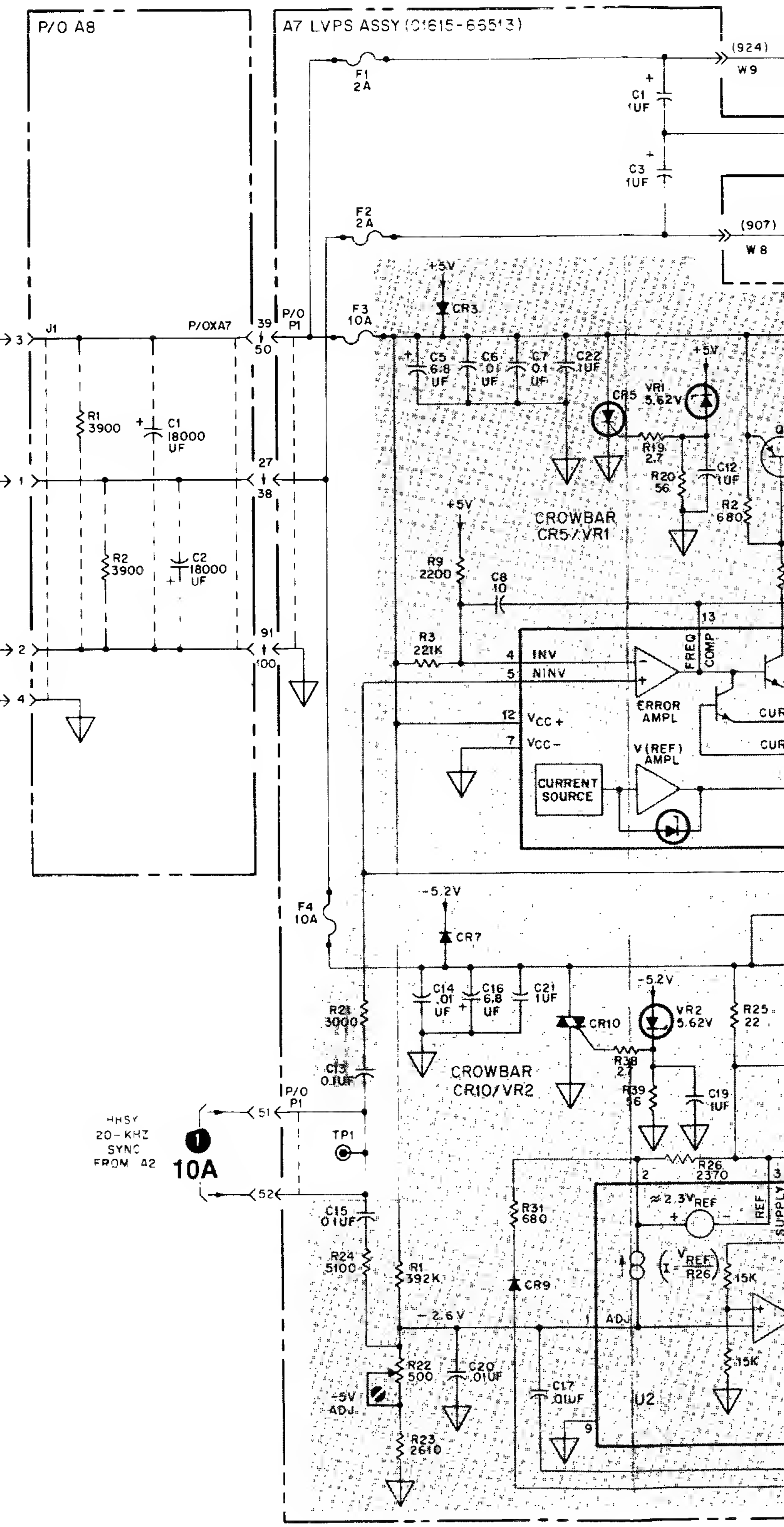
+5-volt Power Supply. The +5-volt supply is a switching regulator with current limiting and over-voltage protection. Pass transistor Q2 in the switching regulator is either saturated or cut off. Therefore, very little power is dissipated in Q2.

Switching Regulator Operation. The 20-kHz sync signal (HHSY) from clock board A2 is converted to a sawtooth wave by A7C13 and A7R21. The reference voltage from pin 6 of U1 is divided by R11, R12, and R18, and added to the sawtooth wave on pin 5 of U1. The error amplifier in A7U1 compares this voltage with the power supply output on pin 4 of U1. That portion of the voltage on pin 5 that exceeds the output voltage on pin 4 turns on the error amplifier. The error amplifier uses a sample of output current from A7R17 to drive a transistor pair which turns on and off current source A7Q1. This controls pass transistor Q2. A7L1, A7CR4, and A7C9 form an averaging network. When Q2 is off, the energy stored in A7L1 draws current from A7C7 and A7C22 provide noise filtering.

+5-volt Supply Protection. If excessive current is drawn from the +5-volt supply, a voltage developed across A7R13 through A7R15 and A7R40 turns on A7Q2. This shunts U1, holding Q2 off until the current has decreased. If excessive voltage develops at the supply output, exceeding the breakdown voltage of A7VR1, A7CR5 will be triggered. A7CR5 shorts the rectifier voltage to ground, opening A7F3.

-5-volt Power Supply. The operation of this supply is very similar to the operation of the +5-volt supply. The voltage developed across A7R26 establishes the value of the reference current through A7R22 and A7R23.

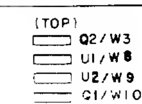


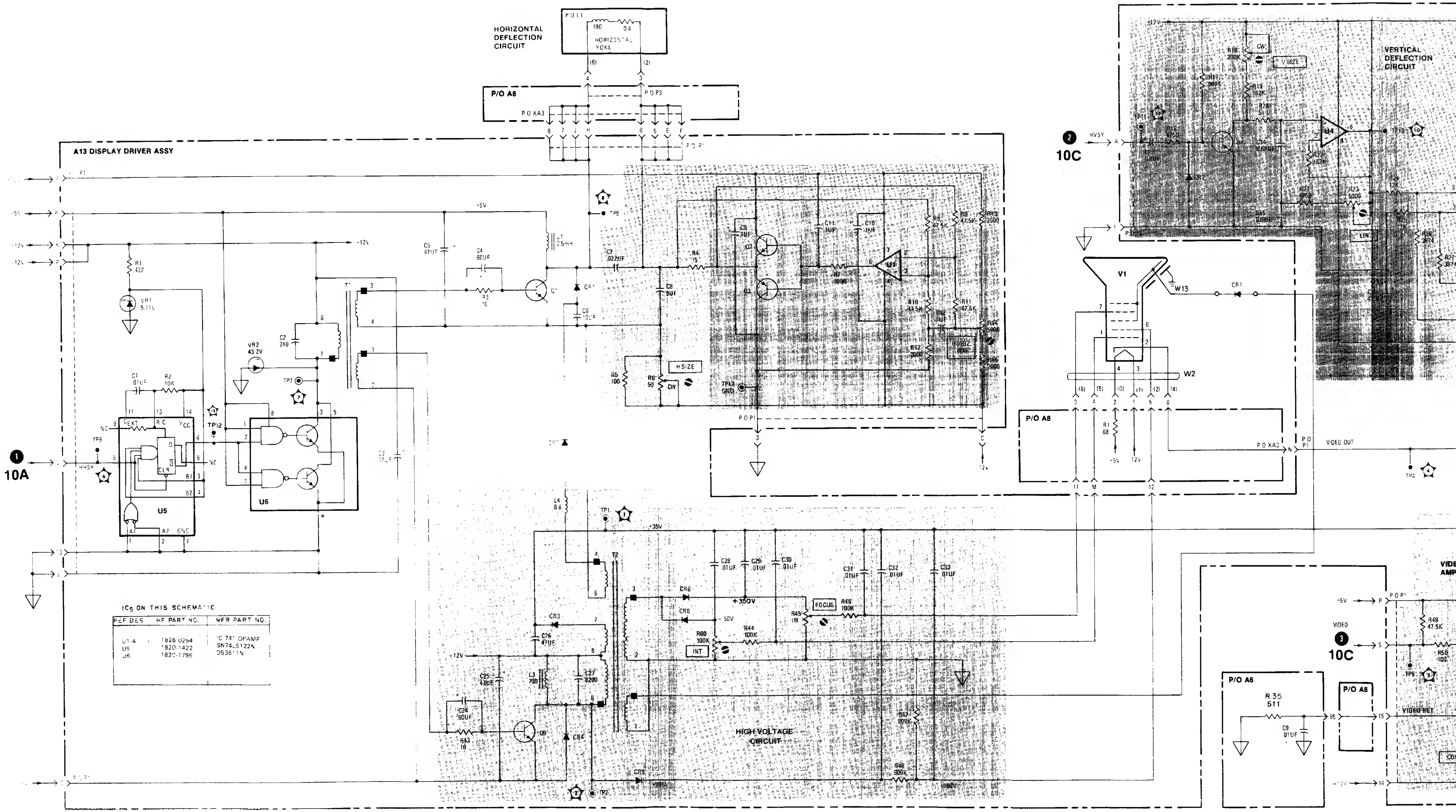


ACTIVE OEVICES ON THIS SCHEMATIC

REF OES	HP PART NO.	MFR PART NO.
A7CR1-3, 6,7,11	1901-0662	MR751
A7CR4	1901-0511	1N3889R
A7CR5	1884-0226	2N6400
A7CR8	1901-0791	1N3889
A7CR9	1901-0040	PG512
A7CR10	1884-0276	MAC15-4
A7Q1	1853-0084	2N4918
A7Q2	1854-0215	2N3904
A7Q3	1854-0300	1854-0300
A7Q4	1853-0036	2N3906
A7U1	1820-0439	UA723
A7U2	1826-0004	LM304H
A7VR1	1902-3096	SZ10939-101
A7VR2	1902-3104	SZ10939-110
CHASSIS		
CR2	1906-0093	MOA3501
Q1	1854-0768	MJE1661
Q2	1854-0768	MJE1661
U1	1826-0221	MC7912CP
U2	1826-0147	MC7812CP

LOCATION OF TRANSISTORS ANO REGULATORS ON REAR PANEL





ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1-4	1826-0254	IC 741 OPAMP
U5	1820-1422	SN74LS122N
U6	1820-1796	DS3611N

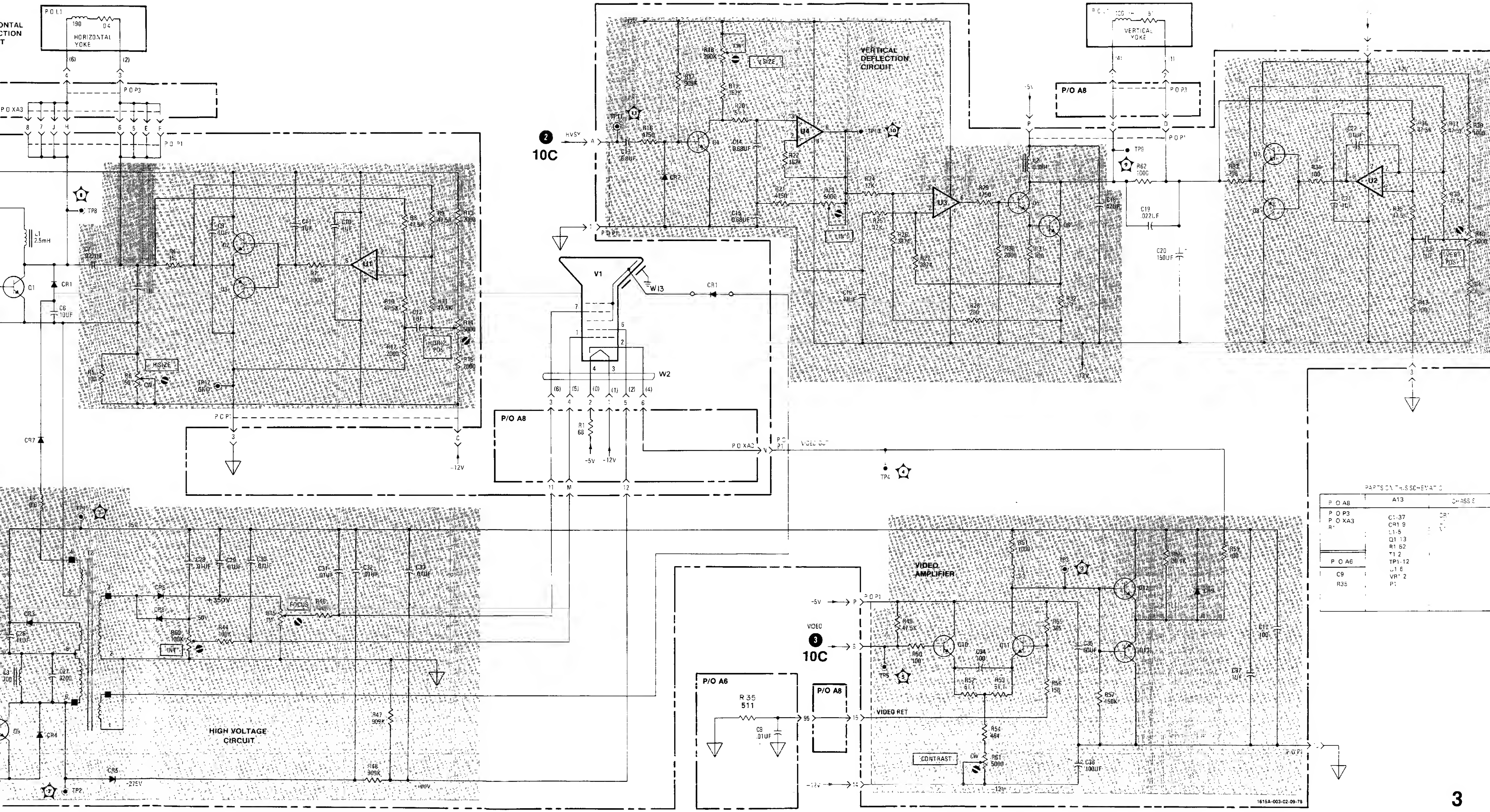


Figure 8-14.
Display Driver (A13) Schematic

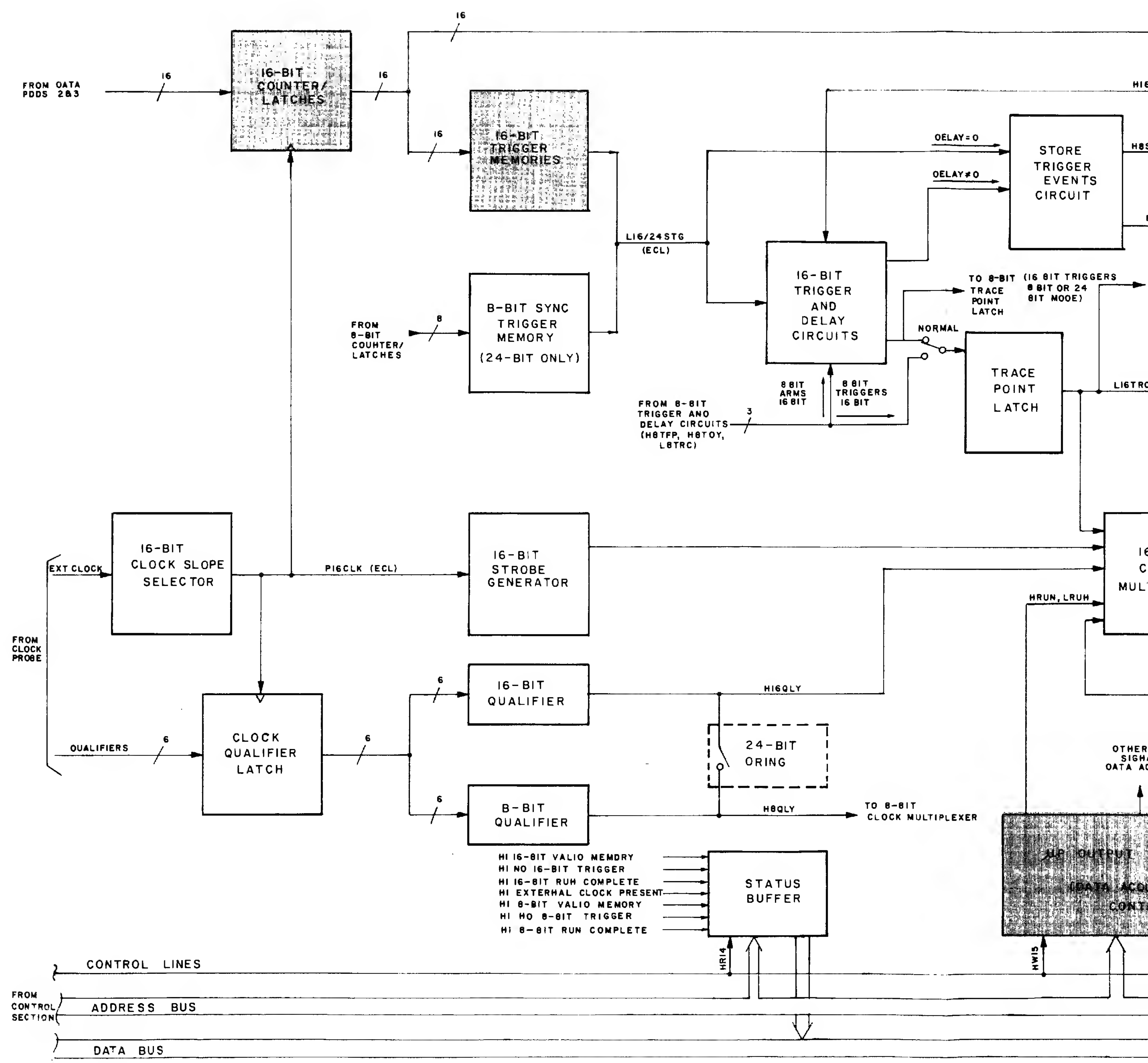
SERVICE SHEET 4A

PRINCIPLES OF OPERATION

The data from the 16 channels of pods 2 and 3 is received by buffers U46A and U49D. These are differential-in/ECL-out line receivers. The line receiver signals are applied to binary counters U31 through U34. The binary counters operate both as latches and as counters. They operate as counters when the software loads the trigger requirements into the trigger memories and during self-test. At all other times, they operate as latches.

Loading of Trigger Memories. When any change is made to a menu, the 1615A software reloads all menu-controlled portions of the instrument prior to the run. The trigger memories are reloaded even if the menu change did not affect trigger requirements. At the start of a run, LMRST (Low Master Reset) switches low. This is inverted through U56A to reset U31 through U34 to binary 0. When LMRST switches high again, the binary counters begin counting P16SCLK(ECL) clocks. The count is applied to the address inputs of the trigger memories. The data to be loaded at each trigger memory address is supplied to pin 13 on U17 and U20. U51C provides the read/write logic for U17 and U20. When the output from U51C is low, the trigger memories load the information on pin 13 data inputs. This information comes from the microprocessor and conforms to the menu selections. The output from U51D is always high except when loading the trigger memories.

Data-acquisition Trace. When a trace starts, LDACQ (Low Data Acquisition) switches low, parallel-enabling U31 through U34 to operate them as latches. They latch data from the line receivers with each P16SCLK(ECL) clock. The latch outputs are supplied both to the trigger memories and to the ECL-to-TTL translators. The trigger memories output an ECL low whenever all memories simultaneously recognize a qualified trigger word on their address inputs. The translators supply their information to the 16-bit data memories shown on service sheet 4C.



clocks. The
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CLK(ECL)
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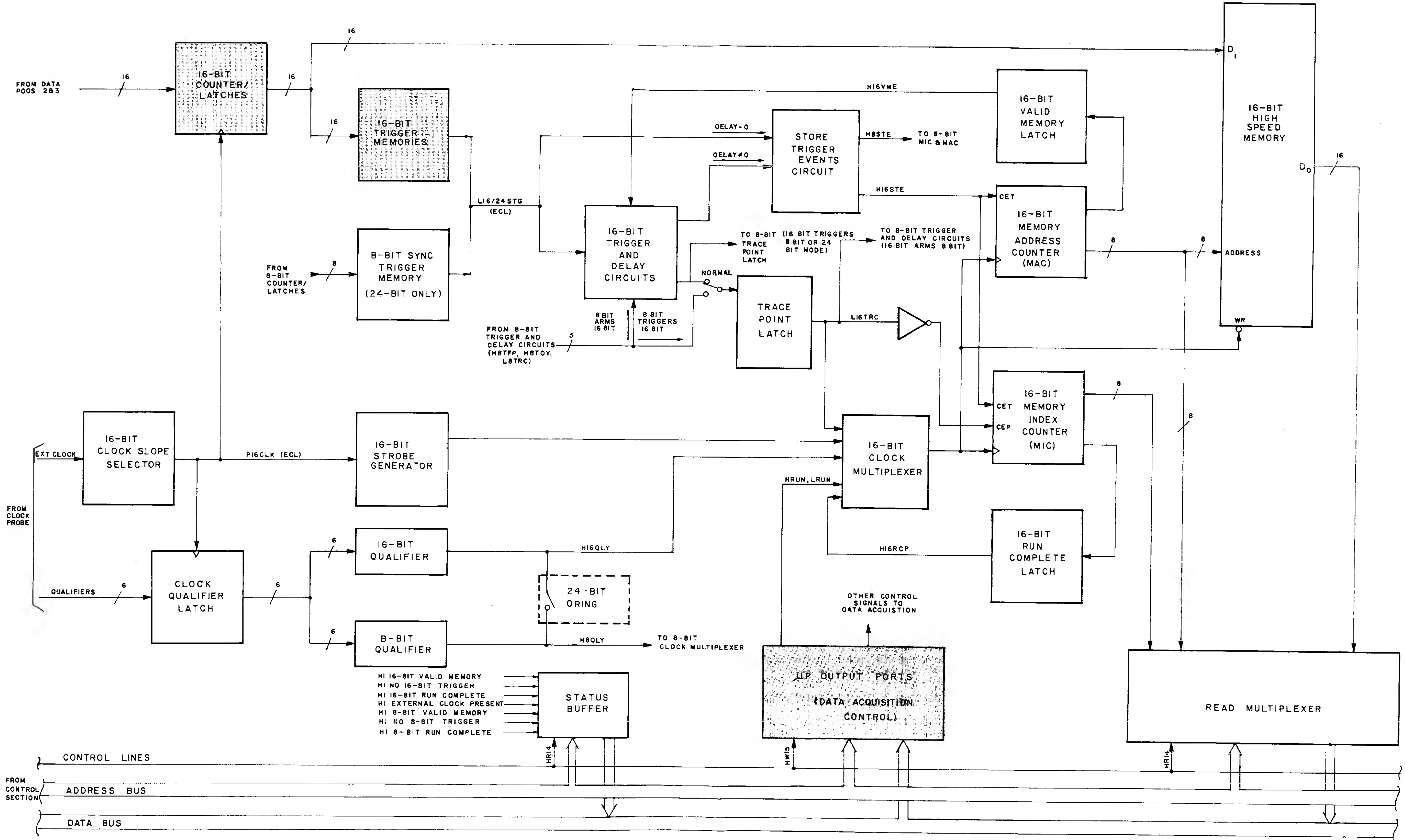
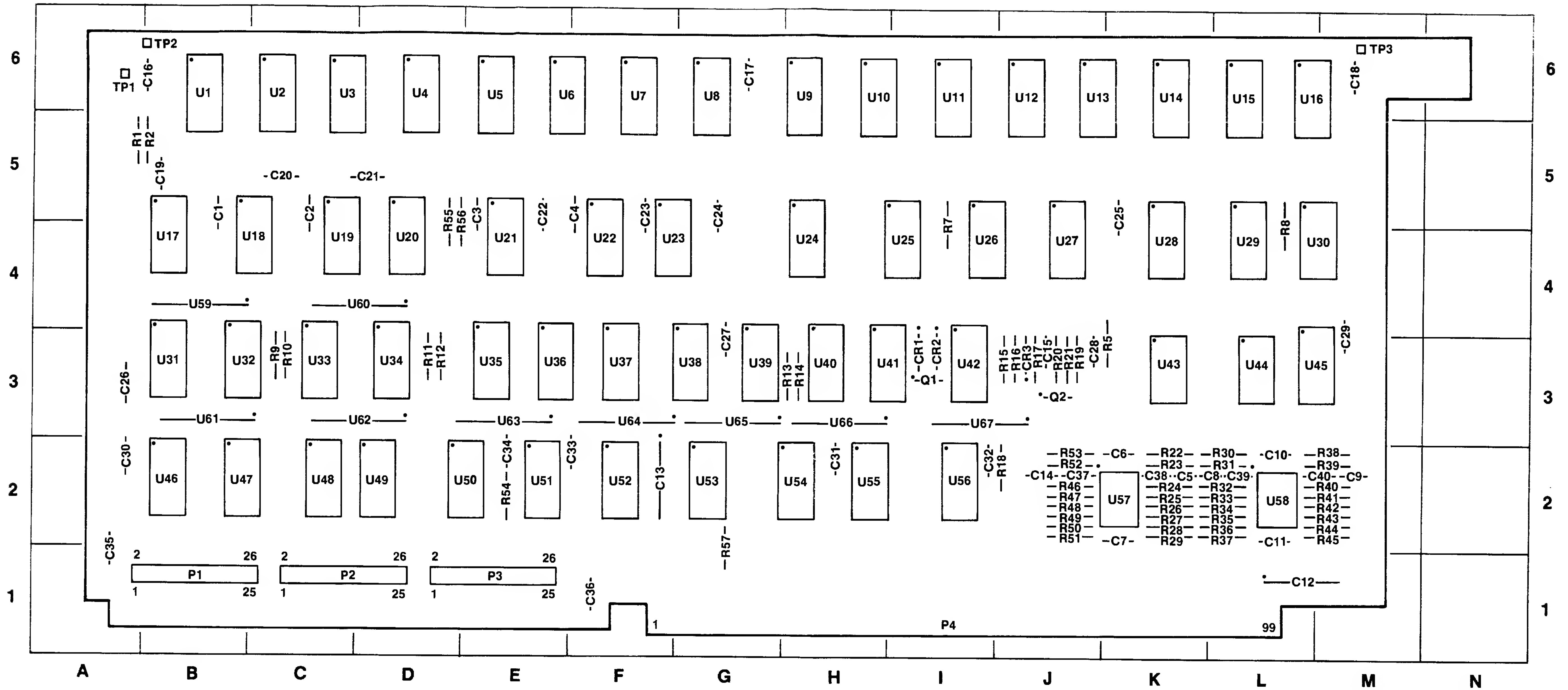
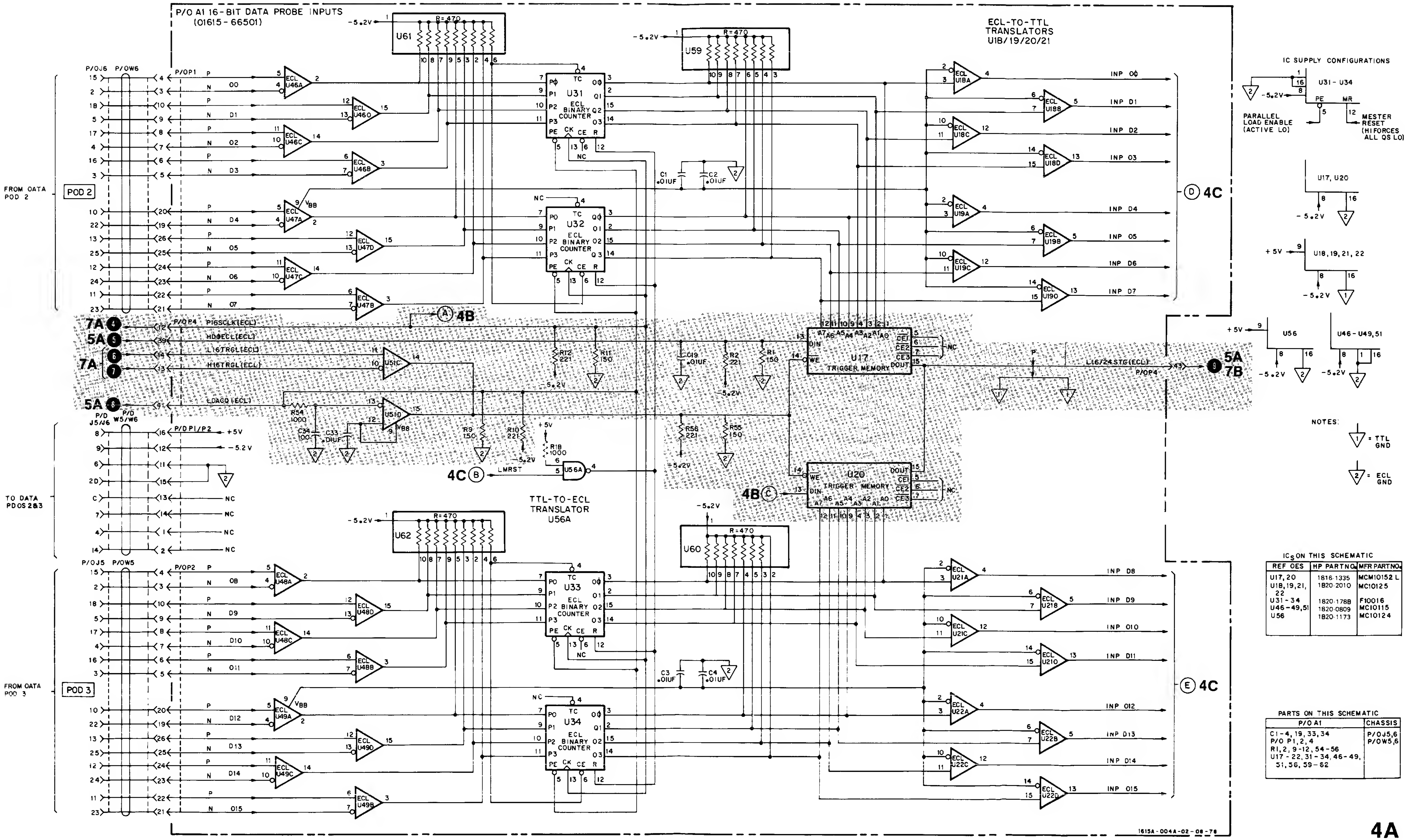


Figure 8-15. Block Diagram, 16-bit Data-acquisition Section for Schematic 4A



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-5	C17	G-6	C33	F-2	R1	A-5	R20	J-3	R36	L-2	R52	J-2	U8	G-6	U23	F-4	U38	G-3	U53	G-2
C2	C-5	C18	M-6	C34	E-2	R2	B-5	R21	J-3	R37	L-2	R53	J-2	U9	H-6	U24	H-4	U39	G-3	U54	H-2
C3	E-5	C19	B-5	C35	A-1	R5	K-3	R22	K-2	R38	M-2	R54	E-2	U10	H-6	U25	I-4	U40	H-3	U55	H-2
C4	F-5	C20	C-5	C36	F-1	R7	I-5	R23	K-2	R39	M-2	R55	D-5	U11	I-6	U26	I-4	U41	H-3	U56	I-2
C5	K-2	C21	D-5	C37	J-2	R8	L-5	R24	K-2	R40	M-2	R56	D-5	U12	J-6	U27	J-4	U42	I-3	U57	K-2
C6	K-2	C22	E-5	C38	K-2	R9	C-3	R25	K-2	R41	M-2	R57	G-2	U13	J-6	U28	K-4	U43	K-3	U58	L-2
C7	K-2	C23	F-5	C39	L-2	R10	C-3	R26	K-2	R42	M-2	T1	A-6	U14	K-6	U29	L-4	U44	L-3	U59	B-4
C8	L-2	C24	G-5	C40	M-2	R11	D-3	R27	K-2	R43	M-2	T2	B-6	U15	L-6	U30	M-4	U45	L-3	U60	D-4
C9	M-2	C25	K-5	CR1	I-3	R12	D-3	R28	K-2	R44	M-2	T3	M-6	U16	L-6	U31	B-3	U46	B-2	U61	B-3
C10	L-2	C26	A-3	CR2	I-3	R13	H-3	R29	K-2	R45	M-2	U1	B-6	U17	B-4	U32	B-3	U47	8-2	U62	D-3
C11	L-2	C27	G-3	CR3	J-3	R14	H-3	R30	L-2	R46	J-2	U2	C-6	U18	C-4	U33	C-3	U48	C-2	U63	E-3
C12	L-2	C28	J-3	P1	B-1	R15	J-3	R31	L-2	R47	J-2	U3	C-6	U19	C-4	U34	D-3	U49	D-2	U64	F-3
C13	F-2	C29	M-4	P2	C-1	R16	J-3	R32	L-2	R48	J-2	U4	D-6	U20	D-4	U35	E-3	U50	E-2	U65	G-3
C14	J-2	C30	A-2	P3	E-1	R17	J-3	R33	L-2	R49	J-2	U5	E-6	U21	E-4	U36	E-3	U51	E-2	U66	H-3
C15	J-3	C31	H-2	Q1	I-3	R18	J-2	R34	L-2	R50	J-2	U6	E-6	U22	F-4	U37	F-3	U52	F-2	U67	I-3
C16	B-6	C32	I-2	Q2	J-3	R19	J-3	R35	L-2	R51	J-2	U7	F-6								

Figure 8-16. State Data-acquisition Assembly A1, Parts Identification



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U17, 20	1816-1335	MCM10152 L
U18, 19, 21, 22	1820-2010	MC10125
U31-34	1820-1788	F10016
U46-49, 51	1820-0809	MC10115
U56	1820-1173	MC10124

PARTS ON THIS SCHEMATIC

P/O A1	CHASSIS
C1-4, 19, 33, 34 P/O P1, 2, 4 R1, 2, 9-12, 54-56 U17-22, 31-34, 46-49, 51, 56, 59-62	P/O J5,6 P/O W5,6

Figure 8-17.
State Data Probe Inputs (P/O A1) Schematic

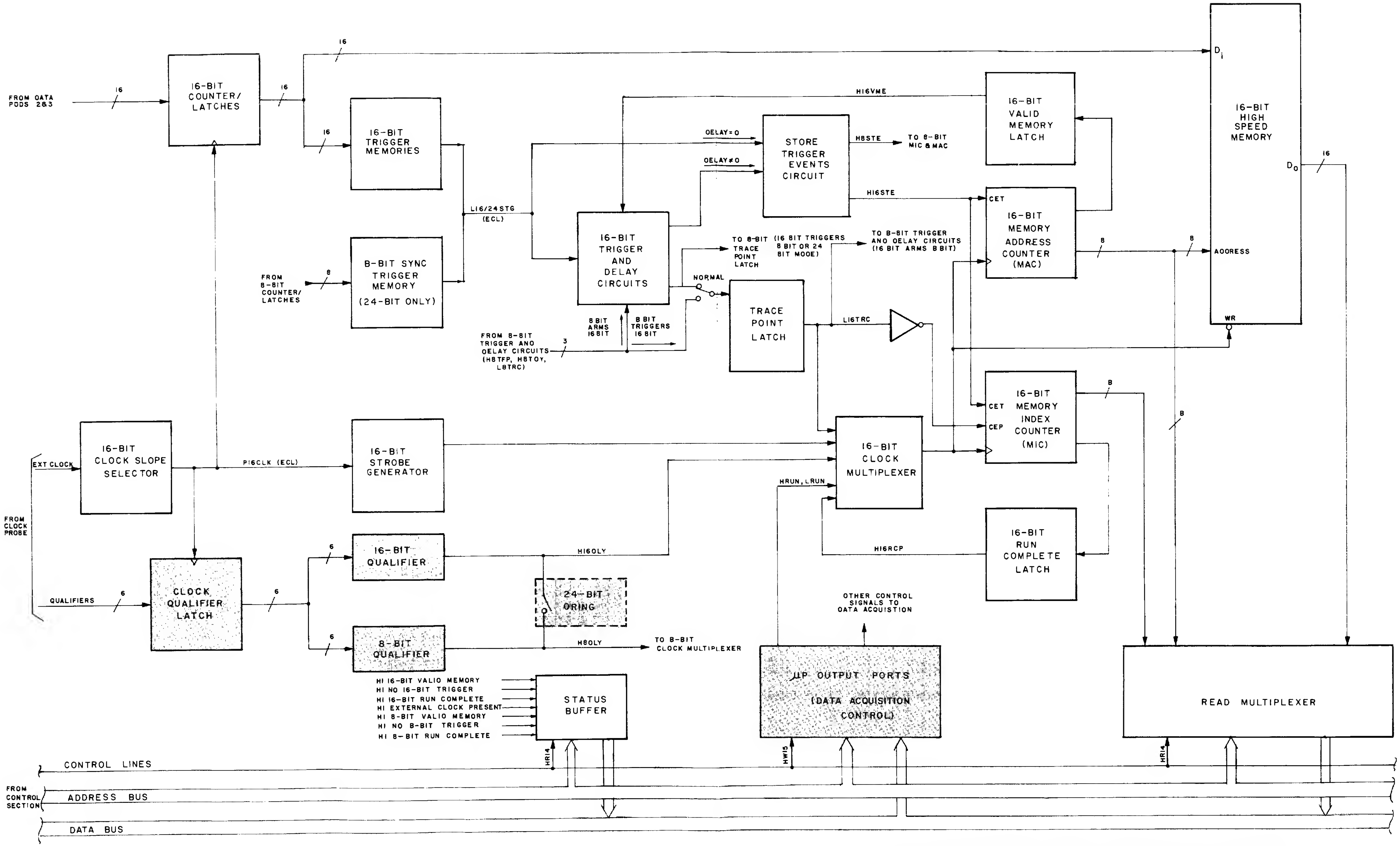


Figure 8-18. Block Diagram, 16-bit Data-acquisition Section for Schematic 4B

SERVICE SHEET 4B

PRINCIPLES OF OPERATION

The qualifier multiplexer consists of two six-bit qualifier words. One of the qualifier words is used for 16-bit qualification, and the other is used for 8-bit qualification. Both words are ORed together for 24-bit qualification. The qualifier words are delivered to logic for ORing or isolation, depending on the trigger mode selected.

There are six qualifier channels in the clock probe. Each qualifier channel is delivered to one bit on both qualifier words. All bits in both words are identical. Only one bit is shown in the simplified qualifier logic diagram.

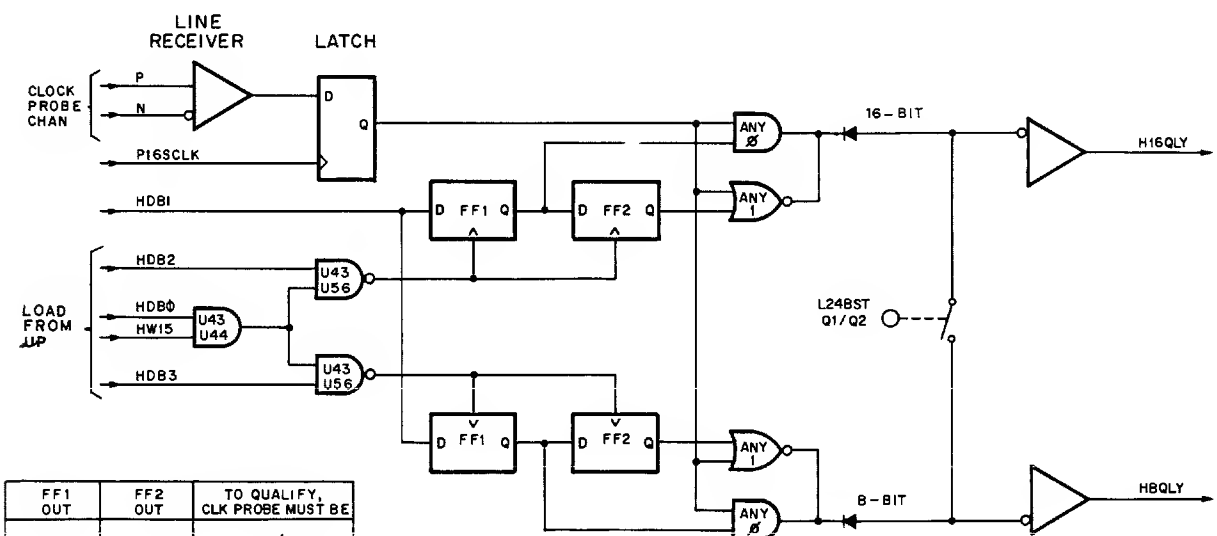
Qualifier Bit Loading. Prior to data acquisition, HW15 and HAB0 enable clocking of the qualifier flip-flops. HDB2 clocks the 16-bit qualifier word. HDB3 clocks the 8-bit qualifier word. The qualifier words are derived from HDB1. The qualifier states establish one of three conditions for qualification: (1) a specific word must occur to obtain qualification, (2) any word will qualify, and (3) no word will qualify.

Qualification Logic. The signal in each qualifier channel is connected through a line receiver and latched with the 16-bit synchronous clock. The latch output is applied to an AND gate and a NOR gate. The AND gate is qualified with any input of 0. The NOR gate is qualified with any input of 1. To select logic 0 to qualify the bit, the microprocessor loads FF1 and FF2 with 1. The NOR gate is satisfied, but the AND gate will only qualify if 0 is latched in from the line receiver. Qualification occurs when all gates supply low outputs. If one gate supplies a high output, it overrides the low from the other gate and prevents qualification (wired OR).

Output Logic (Not 24-bit Mode). L24BST (Low 24-bit State) is high. This saturates Q2 and turns off Q1, isolating the 16-bit and 8-bit qualifier outputs from one another. When qualification occurs in the 16-bit machine, the low across CR1 is applied to U42A and U42D. Two parallel translators are required to drive the load on H16QLY (High 16-bit Qualify). The other inputs of U42A and U42D are connected to ECL threshold. CR3 provides noise margin in the threshold circuit.

Output Logic (24-bit Mode). In the 24-bit mode, L24BST is low, turning off Q2 and saturating Q1. Now CR1 and CR2 OR both qualifiers together. A low state from either qualifier will generate both H16QLY and H8QLY. Both outputs are identical in 24-bit mode (both high or both low). The only time that these signals can be different is in the 16-bit plus 8-bit mode when the 8-bit machine is operating with an external clock or is delaying by an external clock.

When the 8-bit machine is operating with the internal clock and time delay, the 8-bit qualifier is loaded with the DON'T CARE pattern. If only one qualifier word is used in 24-bit mode, the other is loaded with the NEVER pattern.



FF1 OUT	FF2 OUT	TO QUALIFY, CLK PROBE MUST BE
1	1	Ø
Ø	Ø	1
Ø	1	DON'T CARE
1	Ø	NEVER

TRIGGER MODE	1615A MONITORS FOR QUALIFICATION
16 ARMS/TRIGS 8	H16QLY
8 ARMS/TRIGS 16	H8QLY
24-BIT (L24BST)	H16QLY (OR) H8QLY

SIGNATURE ANALYSIS FOR SCHEMATIC 4B.

The signatures on this schematic are obtained by using DSA Setups A and D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A1 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A1, and install A1 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ↓
STOP.................................... ↑
CLOCK.................................. ↓

Signatures for DSA Setup A (Schematic 4B)

Pin	Signature
VH A1U1-16	C690
A1U43-5	FHPA
A1U43-10	AHA3
A1U43-12	08F5
A1U56-7	57CA

DSA SETUP D.

1. Remove assembly A1 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A1 and install A1 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   c. Connect signature analyzer stop line to same point as start line, step b above.

   d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{\text{WR}}$ line.

4. Reinstall A5 in 1615A mainframe.

NOTE

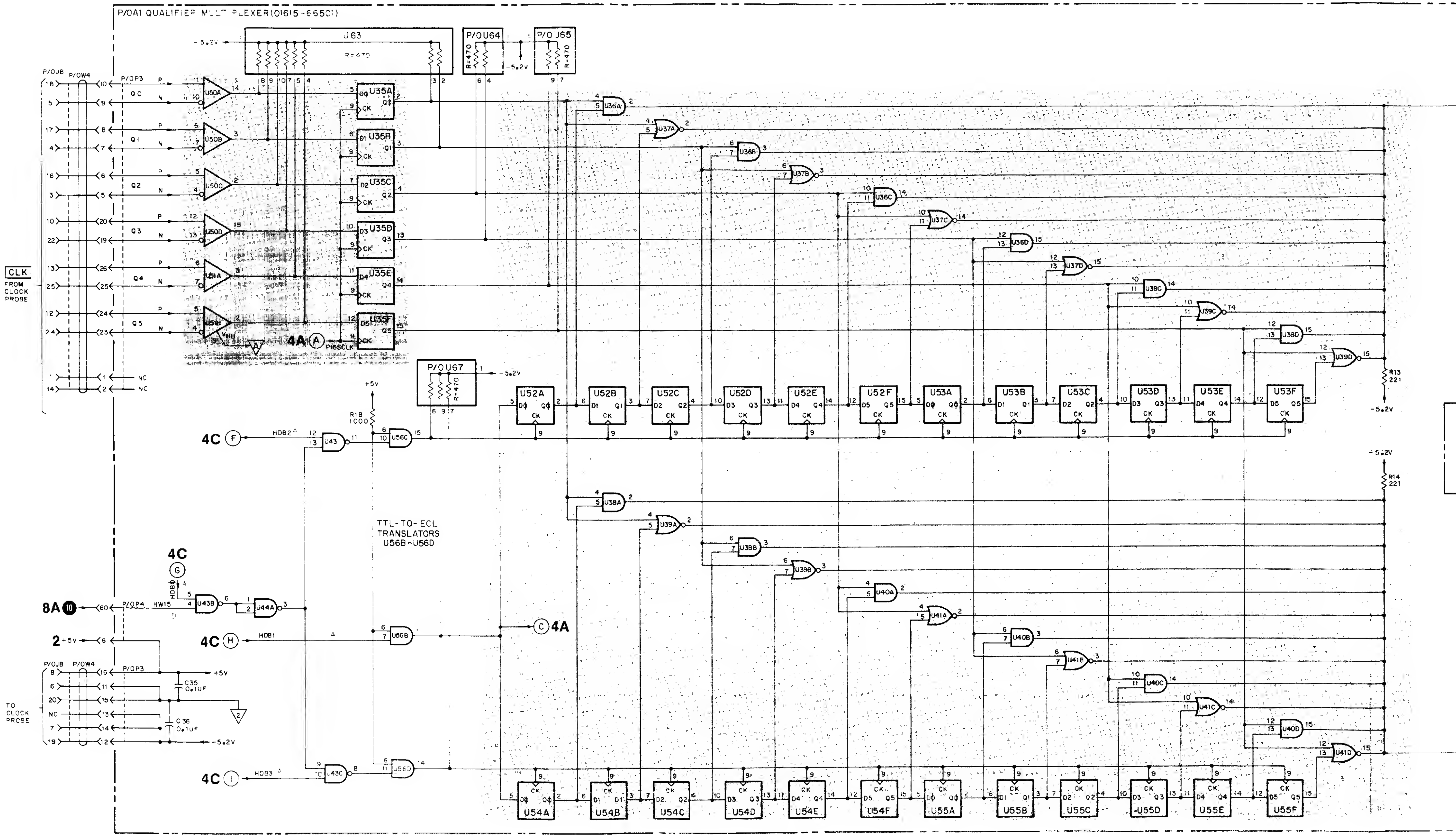
DSA jumper on A5 remains in NM (normal) position in this test setup.

5. Set up signature analyzer as follows:

START .... ↑
STOP.................................... ↑
CLOCK.................................. ↑

Signatures for DSA Setup D (Schematic 4B)

Pin	Signature
VH A1U1-16	0001
A1U43-4	0000 (blinking)


P/OA1 QUALIFIER MULTIPLEXER(01615-66501)
U63
R=470
P/OU64
P/OU65
CLK
FROM CLOCK PROBE
TO CLOCK PROBE
P/OJB
P/OW4
P/OP3
Q0
Q1
Q2
Q3
Q4
Q5
U50A
U50B
U50C
U50D
U51A
U35A
U35B
U35C
U35D
U35E
U35F
4A
P16SCLK
P/OU67
R18 1000
+5V
-5.2V
4C
HDB2
U43
U56C
TTL-TO-ECL TRANSLATORS U56B-U56D
8A
P/OP4
HW15
U43B
U44A
2
4C
HDB1
U56B
4A
C35 0.1UF
C36 0.1UF
4C
HDB3
U43C
U56D
U36A
U37A
U36B
U37B
U36C
U37C
U36D
U37D
U38C
U39C
U38D
U39D
R13 221
R14 221
U52A
U52B
U52C
U52D
U52E
U52F
U53A
U53B
U53C
U53D
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U41C
U40D
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U55D
U55E
U55F

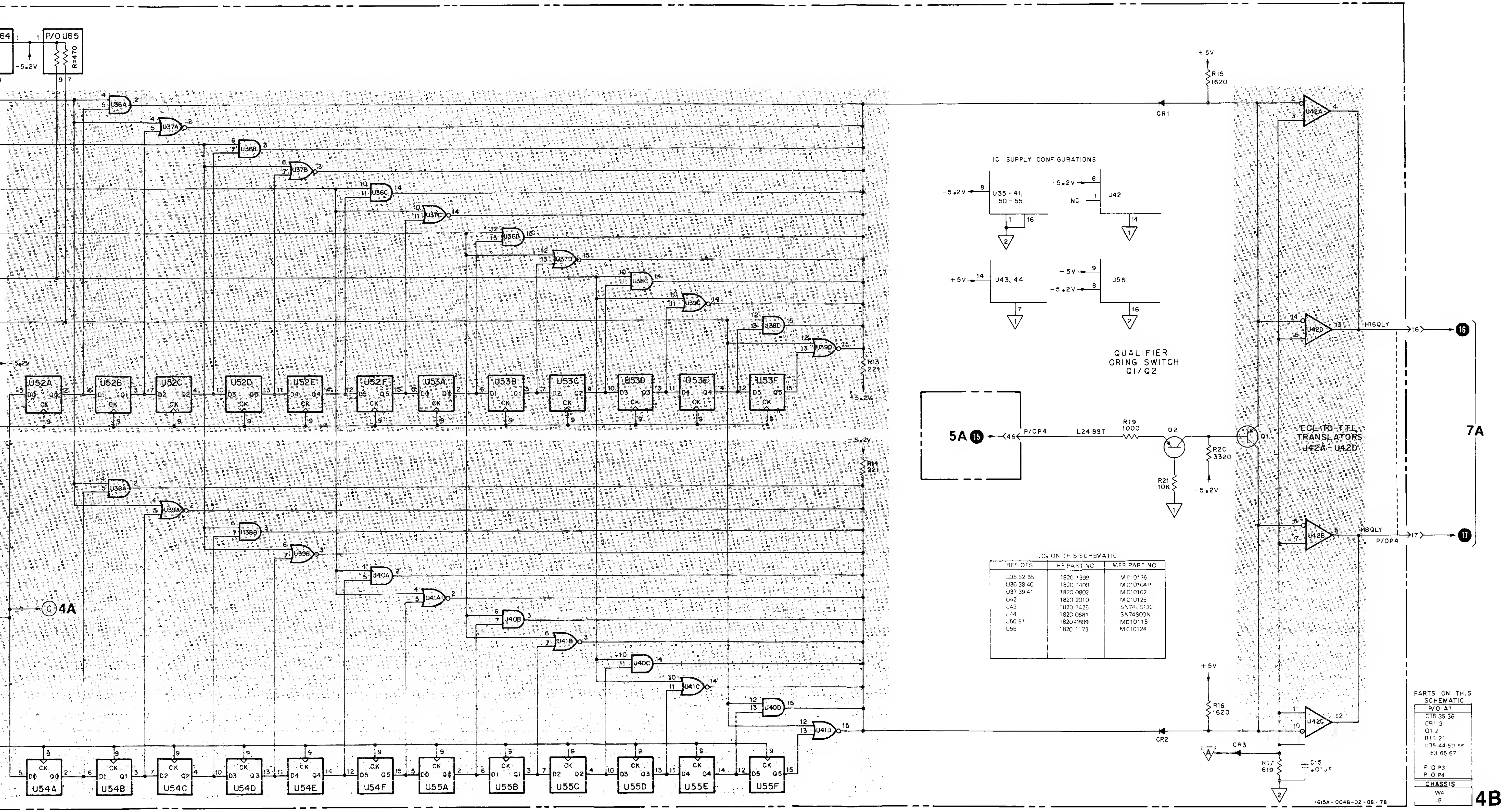


Figure 8-19.
Qualifier Multiplexer (P/O A1) Schematic

SERVICE SHEET 4C

PRINCIPLES OF OPERATION

16-bit Memory. U1 through U16 comprise the 16-bit memory. Each chip is a 256X1 binary memory. The 16 chips of memory are addressed by memory address counter U29 and U30. Data which enters the 16 channels shown on schematic 4A is supplied to the 16 channels of memory. After a short delay which allows data to stabilize, L16MWRT (Low 16-bit Memory Write) from A2 enables all memory chips simultaneously for about 30 nanoseconds. They accept the 16 channels of data. At the end of L16MWRT, the memories are returned to the read state and the memory address counters are advanced to the next sequential address by P16CCLK (16-bit Counter Clock).

Output Selector. U23, U24, U27, and U28 comprise an output selector. The selector allows the microprocessor to obtain the state of the memory address counter or the memory index counter, or to obtain the digital information for bits 1 through 8 or for bits 9 through 16 from memory. One of these four selections is made by decoding HAB0 and HAB1 from the microprocessor address bus. U43A decodes HR14 and HAB4 to either place the selected output on the data bus or set the selector chips in the high impedance state when their information is not desired.

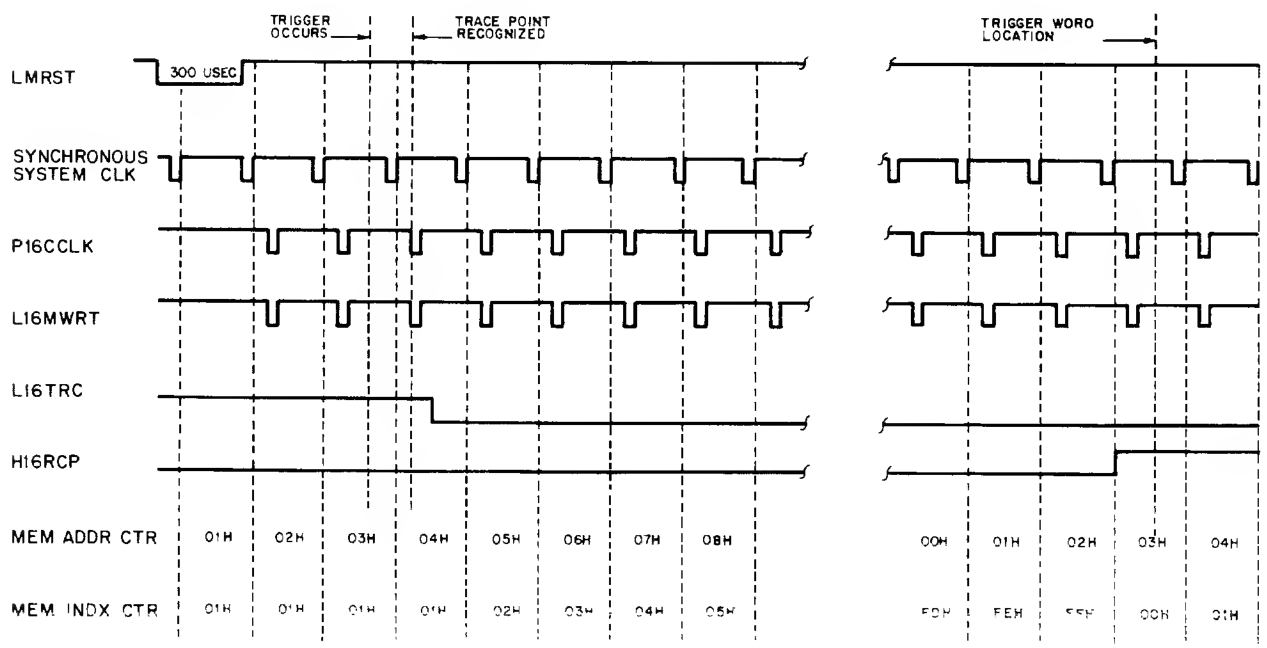
Memory Address Counter. The memory address counter is a count-up counter. It counts from 0 to 255, continuously. Its count addresses specific locations within the 16 memory chips.

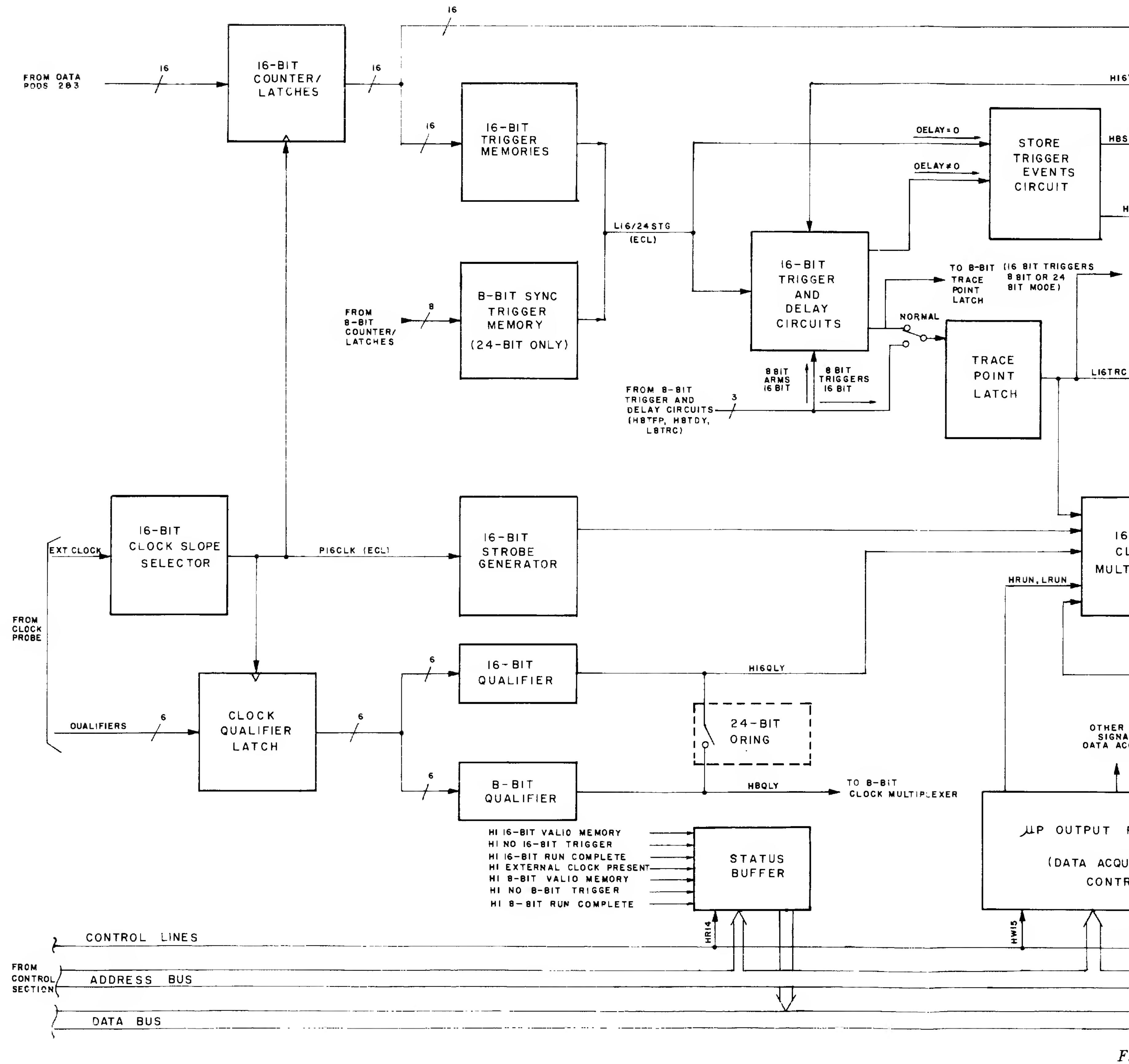
Memory Index Counter. The purpose of the memory index counter is to stop data acquisition when the 16-bit memory is full of valid data and to indicate the portion of memory that is valid when only a partial run has taken place. The memory index counter is only used in modes where the trigger starts data acquisition. In modes where the trigger ends data acquisition, trigger recognition stops the run and the memory index counter is not needed.

DATA-ACQUISITION RUN WITH TRIGGER STARTS TRACE. (See waveform diagram.)

Before the Run Starts. When the TRACE key is pressed, the microprocessor sets LMRST (Low Master Reset) low for approximately 300 microseconds. During this period, the memory address counter and memory index counter are parallel loaded to binary 1, and clocks are prevented from reaching the two counters. Low states are forced on H16RCP (High 16-bit Run Complete) and H16VME (High 16-bit Valid Memory) to remove the valid-memory and run-complete indications.

Memory Address Counter Begins. When LMRST switches high, it releases the counters and the flip-flops





ss counter
5, continu-
within the

e memory
the 16-bit
portion of
has taken
l in modes
In modes
er recogni-
nter is not

STARTS

is pressed,
Reset) low
his period,
ex counter
prevented
e forced on
H16VME
d-memory

LMRST
e flip-flops

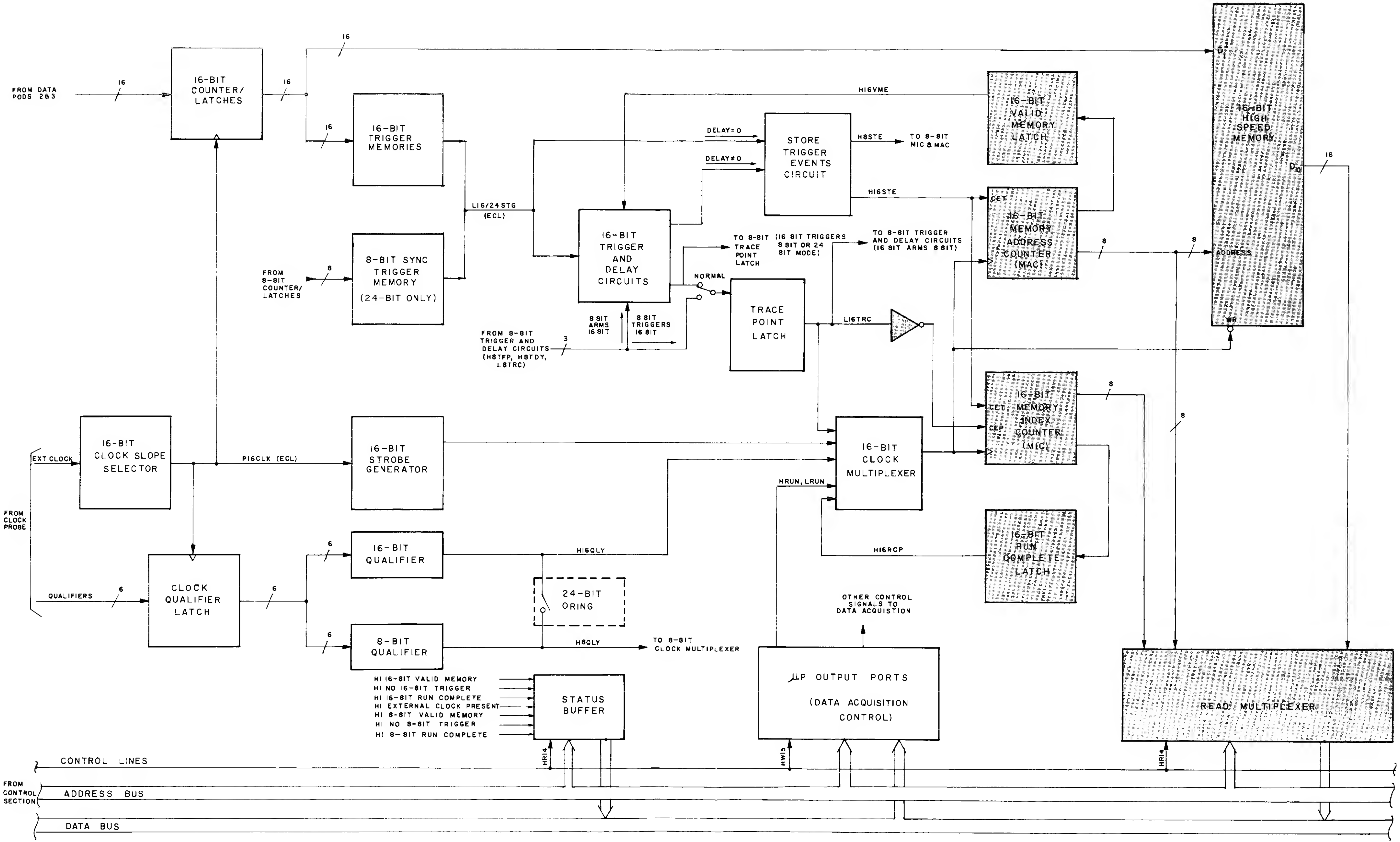


Figure 8-20. Block Diagram, 16-bit Data-acquisition Section for Schematic 4C

and allows the P16CCLK clocks to enter. U45A is immediately set through U44C, providing a high H16VME, but H16RCP remains low. H16STE (High 16-bit Store Trigger Events) is always high, except during trace events mode. In trace events mode, H16STE is only high during clock periods which include a recognized trigger. Although the memory address counter begins counting P16CCLK clocks, the memory index counter is held off by a high L16TRC (Low 16-bit Trace Point). L16MWRT clocks arrive at the same time that P16CCLK clocks arrive. L16MWRT clocks enter the 16-bit data word into memory. Then the memory address counter is incremented to the next sequential address, and the next 16-bit data word is entered into memory. This continues with each arrival of the P16CCLK and L16MWRT clocks.

Memory Index Counter Begins. When the trace point is recognized (trigger plus delay specification met in the 16-bit machine), L16TRC switches low. The output of U44B switches high, enabling the memory index counter. The memory index counter begins counting P16CCLK clocks. There is a delay between P16CCLK and L16TRC to ensure that the memory index counter does not count the period which included L16TRC. The trigger word enters the memory location corresponding to count 0 in the memory index counter.

Data-acquisition Halts. The memory index counter advances to binary 255 and generates terminal count. The terminal count is NANDed with H16STE. When both signals are high, signifying a full memory of valid data, the $\overline{K}$ input of U45B goes low. U45B generates H16RCP (High 16-bit Run Complete) when the next P16CCLK arrives. H16RCP is supplied to the clock assembly A2 where it halts P16CCLK and L16MWRT.

Microprocessor-controlled Display. Since the memory index counter began its count at binary 1 and issued terminal count at 255, the memory address counter will stop at the address which contains the trace point (the trigger word if the menu selection was 0 delay). Now the microprocessor can provide a display referenced to the location of the trigger word. The trigger word is assigned line number 000 on the display, with all subsequent words assigned higher line numbers. To display other locations in memory, the microprocessor supplies clocks to the memory address counter. The microprocessor supplies one clock for each higher address line desired, and 255 clocks (the reciprocal of 1) for each lower address line desired. If the operator selects line 127 in memory, the microprocessor will supply 127 clocks to the memory address counter to increment to the desired memory address. Then if the operator elects to see line 126, the microprocessor will supply 255 clocks to increment the memory from line 127 to line 126.

The microprocessor reads bits 0 through 7 and then bits 8 through 15 at each memory location in order to present the display.

Data-acquisition Run with Trigger Ends Trace. This mode of operation is nearly the same as the START trace mode. The major difference rests in the fact that the memory index counter is not used in this mode, and H16VME is used. In the START trace mode, the memory index counter signals the end of data acquisition. In the END trace mode, recognition of the trace point (L16TRC) ends data acquisition. H16VME must be high before the 1615A can recognize L16TRC.

Data-acquisition Phase. In the END trace mode, H16START is low. When the TRACE key is pressed, the memory address counter begins at count 1 and starts advancing with P16CCLK clocks. H16VME is low because U45A is reset at the beginning of data acquisition. The low H16VME is interpreted as memory incomplete. It prevents the 1615A from recognizing its trace point. When the memory address counter reaches terminal count, the J input of U45A receives a high state. With arrival of the next P16CCLK, H16MVE is clocked high. It remains high for the rest of the run, indicating that the memory has been filled with valid data. Now the 16-bit machine is free to recognize trace point. When trace point is recognized, the 1615A cuts off P16CCLK and L16MWRT clocks, stopping data acquisition.

Display Phase. Since the memory address counter began its count at binary 1, there is one doubtful location in memory: binary 0. In END trace modes, after trace point has been recognized, the microprocessor reads the address of the memory address counter. If the address is not 0, then the microprocessor determines that all memory locations contain valid data. If the address is 0, then data in location 0 may not be valid. In this case, the software prevents display of the data contained in location 0.

Partial Runs. Partial runs can occur if the system clock is lost or the operator presses the STOP key before the trace point has been recognized in the END trace mode. When a partial run occurs in the END trace mode, the microprocessor will read H16VME to determine if 255 valid words have been captured in memory. If H16VME is low, the microprocessor will read the address from the memory address counter to determine how many lines in memory were captured before the STOP key was pressed. Then the software will allow only that number of lines to be displayed, and will blank all of the other memory locations.

If H16VME is high, then at least 255 valid words have been captured in memory. In this case, the microprocessor will check the address to see if it is location 0. It not location 0, then all 256 memory locations contain valid data. If the address is location 0, then only 255 locations will be displayed and location 0 will be blanked.

When a partial run occurs in START trace mode, the microprocessor will read the address of the memory index counter. By reading the memory index counter, the microprocessor determines how much of the memory contains valid data, and permits display of only that portion of memory.

Slow Clock Runs. The microprocessor also reads the memory index counter when a run is in process and a very slow clock is in use. In this case, the display informs the operator of how many valid words have been captured into memory as the run progresses.

SIGNATURE ANALYSIS FOR SCHEMATIC 4C.

The signatures on this schematic are obtained by using DSA Setups A and C. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A1 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A1, and install A1 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ‾|_
STOP.................................... _|‾
CLOCK.................................. ‾|_

Signatures for DSA Setup A (Schematic 4C)

Pin	Signature	Pin	Signature
VH A1U23-7	FHPA	A1U27-7	C43H
A1U23-9	57CA	A1U27-9	C6P3
A1U24-7	08F5	A1U28-7	FA2P
A1U24-9	AHA3	A1U28-9	427H

DSA SETUP C.

1. Remove assembly A1 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A1 and install A1 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   d. Connect signature analyzer stop line to same point as start line, step b above.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 part number is 01615-66505). This is the DBIN line from the microprocessor.

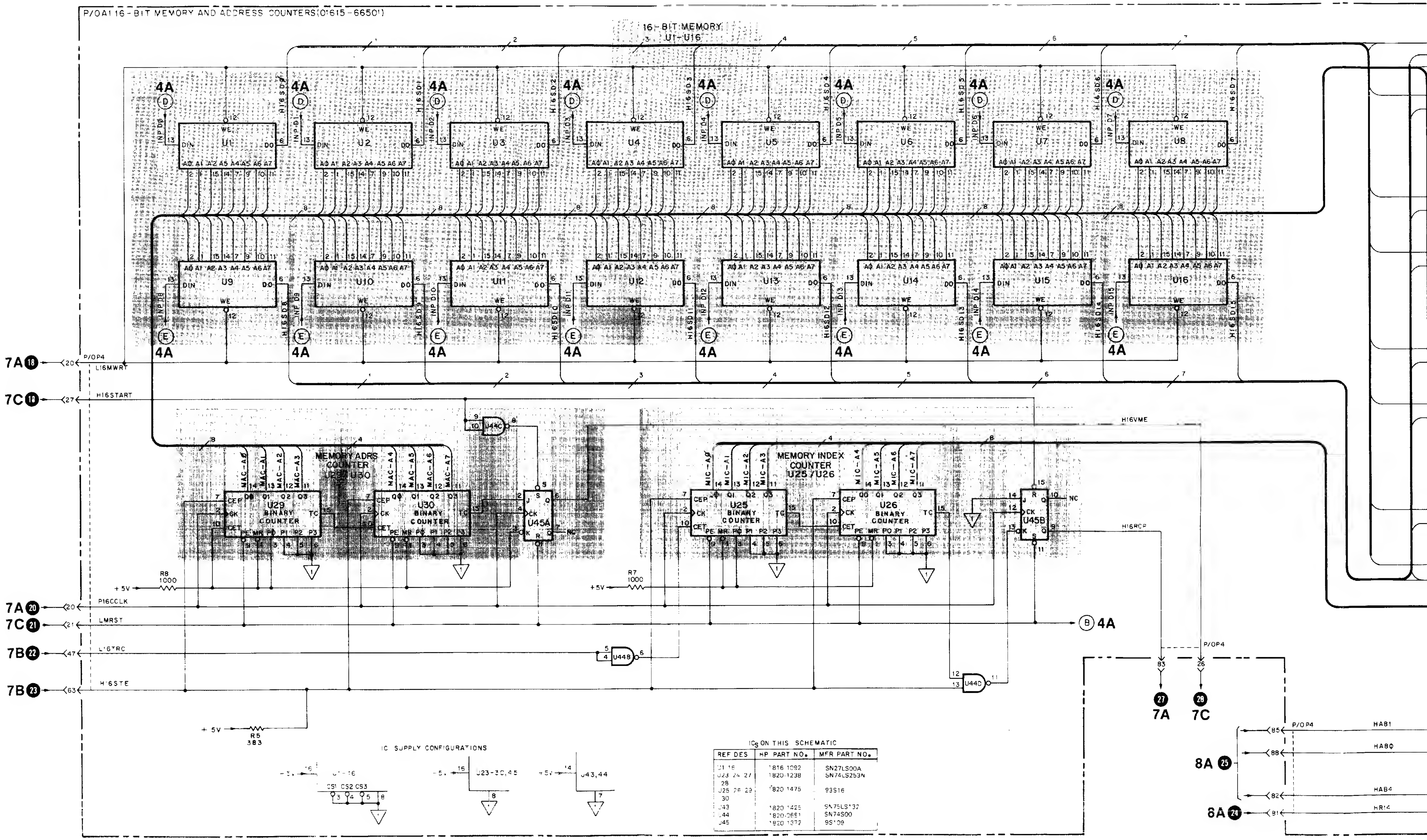
4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... _|‾
STOP.................................... _|‾
CLOCK.................................. ‾|_

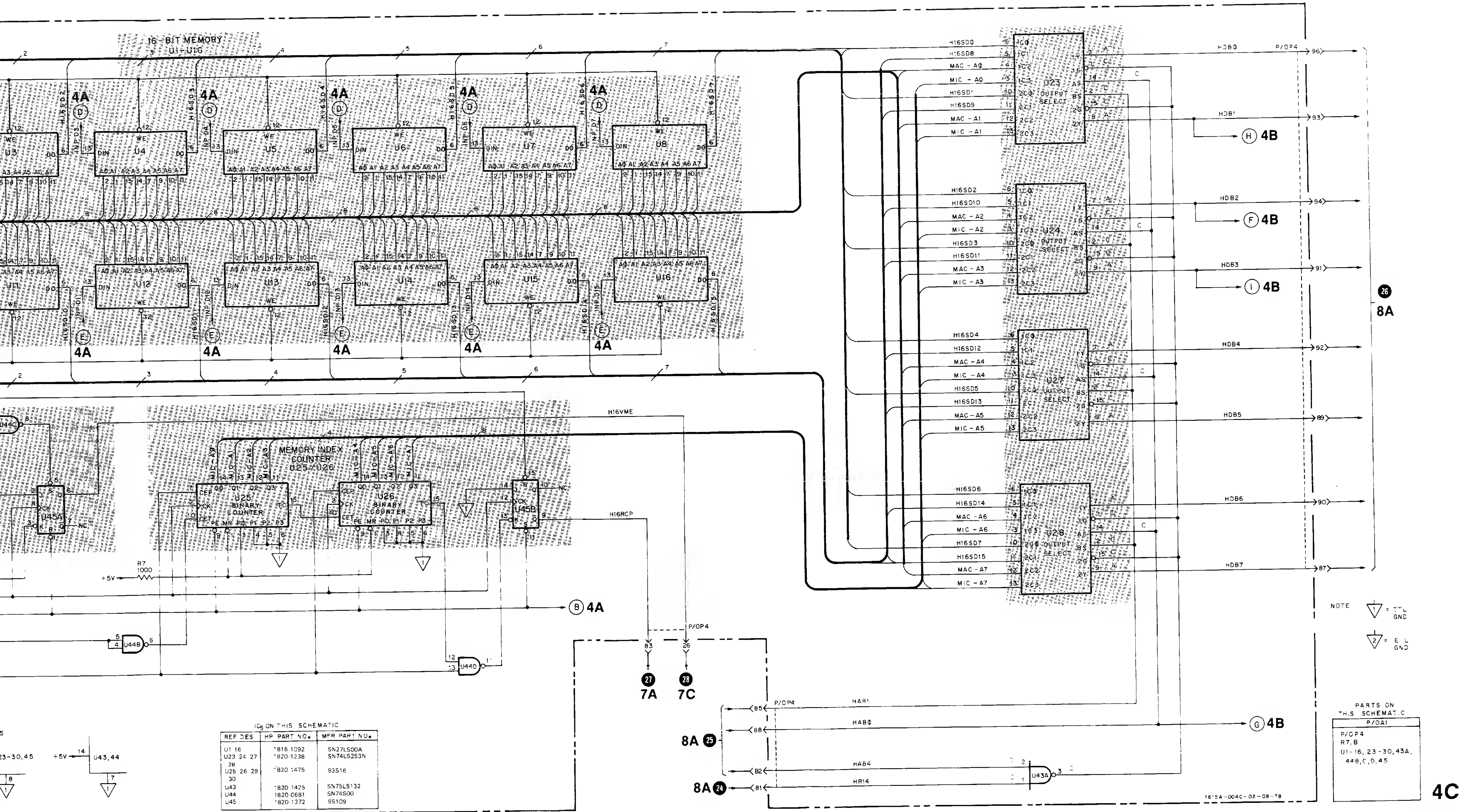
Signatures for DSA Setup C (Schematic 4C)

Pin	Signature	Pin	Signature
VH A1U1-16	0001	A1U27-2	5555
A1U23-1	95F3	A1U27-14	UUUU
A1U23-2	5555	A1U27-15	95F3
A1U23-14	UUUU	A1U28-1	95F3
A1U23-15	95F3	A1U28-2	5555
A1U24-1	95F3	A1U28-14	UUUU
A1U24-2	5555	A1U28-15	95F3
A1U24-14	UUUU	A1U43-1	3827
A1U24-15	95F3	A1U43-2	5H21
A1U27-1	95F3	A1U43-3	95F3



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1-16	1816-1092	SN27LS00A
U23, 24, 27, 28	1820-1238	SN74LS253N
U25, 26, 29, 30	1820-1475	93S16
U43	1820-1425	SN75LS132
U44	1820-0681	SN74S00
U45	1820-1372	9S109



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1 16	1816 1092	SN27LS00A
U23 24 27 28	1820-1238	SN74LS253N
U25 26 29 30	1820 1475	93S16
U43	1820 1425	SN75LS132
U44	1820-0681	SN74S00
U45	1820-1372	9S109

Figure 8-21.
State Memory and Address Counter (P/O A1) Schematic

SERVICE SHEET 4D

PRINCIPLES OF OPERATION

There are four independent threshold drivers in the 1615A, one for each probe pod. This prevents threshold errors due to ground differences between pods. There are only three threshold voltage selectors in the 1615A: one for the clock probe, one for the 8-bit data pod, and one for the combined 16-bit data pods. Isolation is sufficient between the threshold drivers so that a failure occurring in one threshold driver may not affect the operation of any other threshold driver.

The four threshold drivers are identical. Only one will be discussed. U58C and U58D form an amplifier stage with a gain of -0.2 (divide by 5). R38 isolates U58D from the capacity of the probe cable, and provides for matching the offset currents of the comparators inside the probe pod. C9 provides low frequency rolloff in the threshold amplifier. C40 protects U58 against high frequency transients.

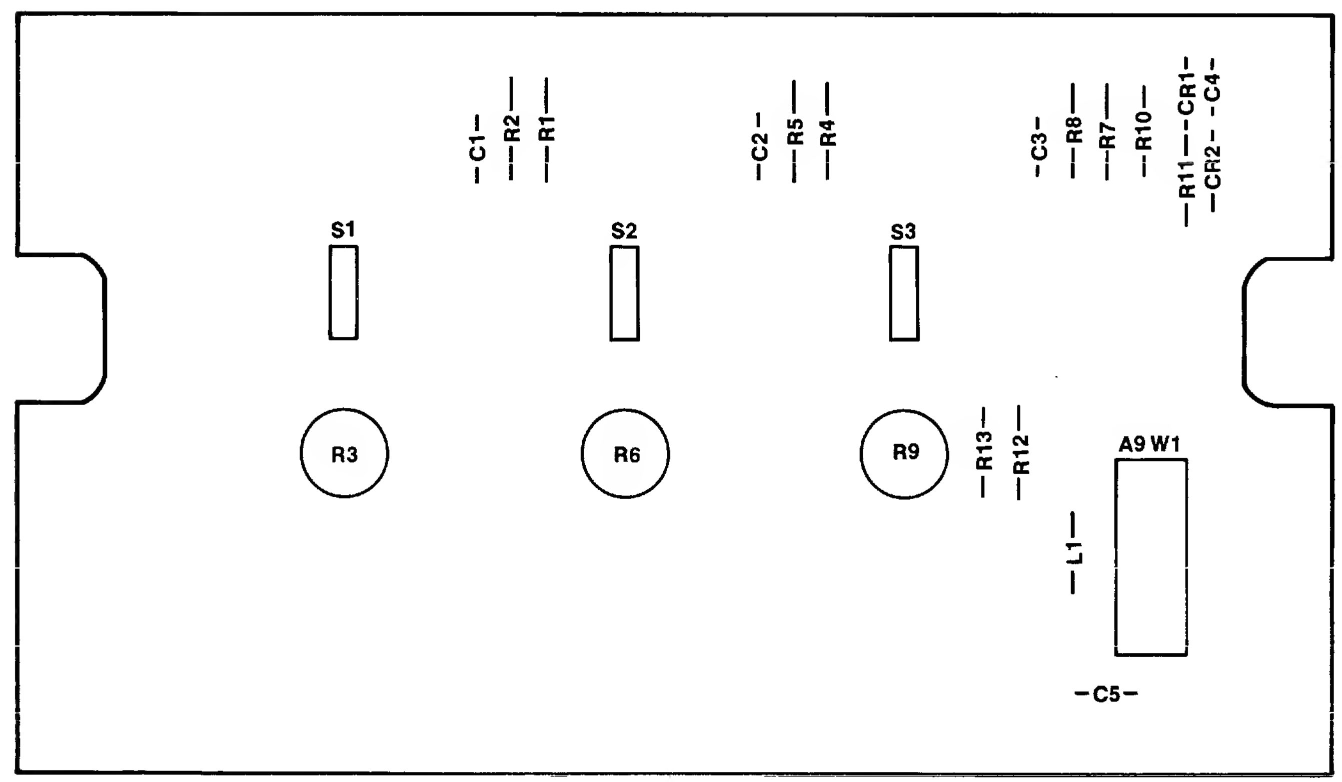


Figure 8-22. Probe Threshold/Input Assembly A9, Parts Identification

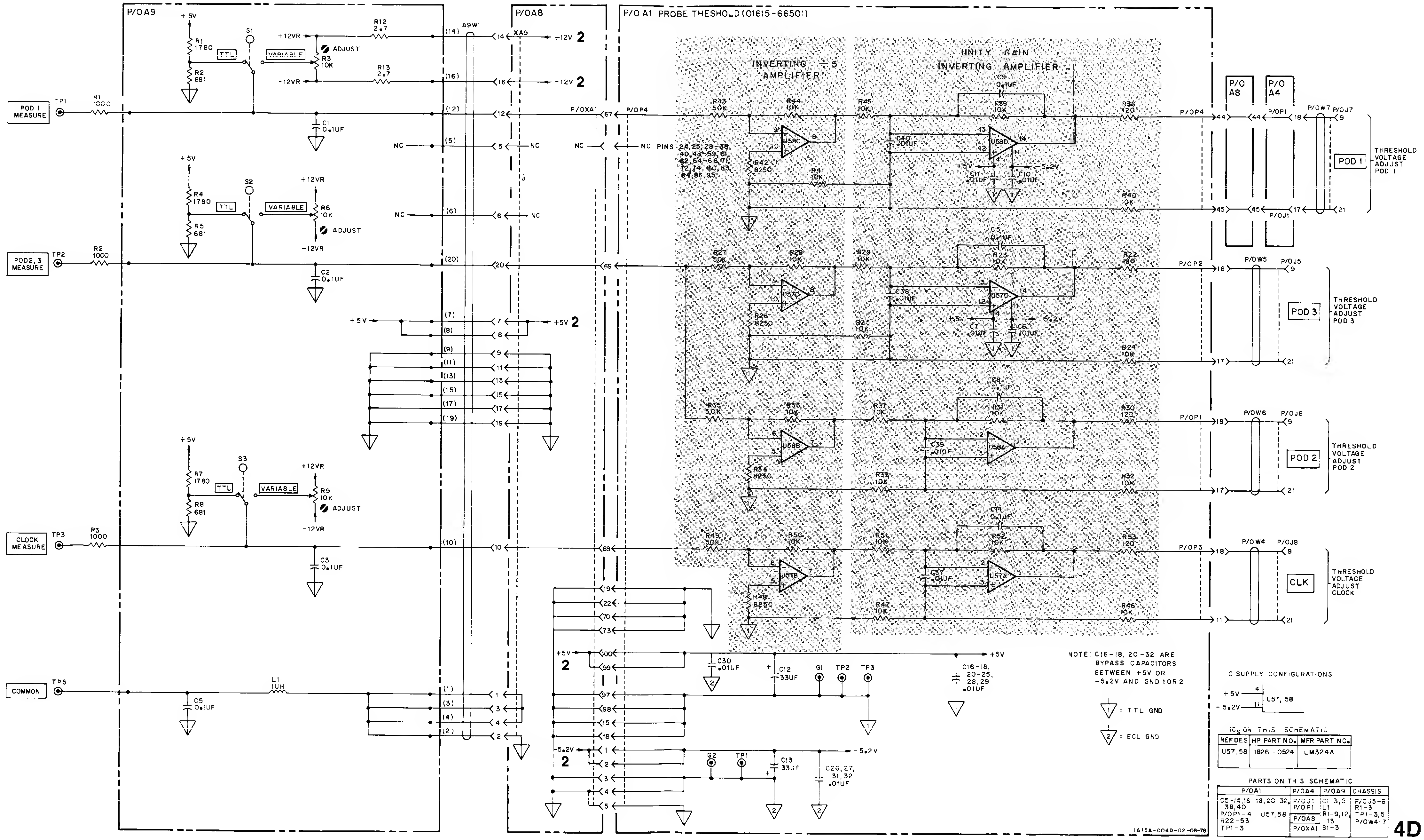


Figure 8-23.
Probe Thresholds (A9 and P/O A1) Schematic

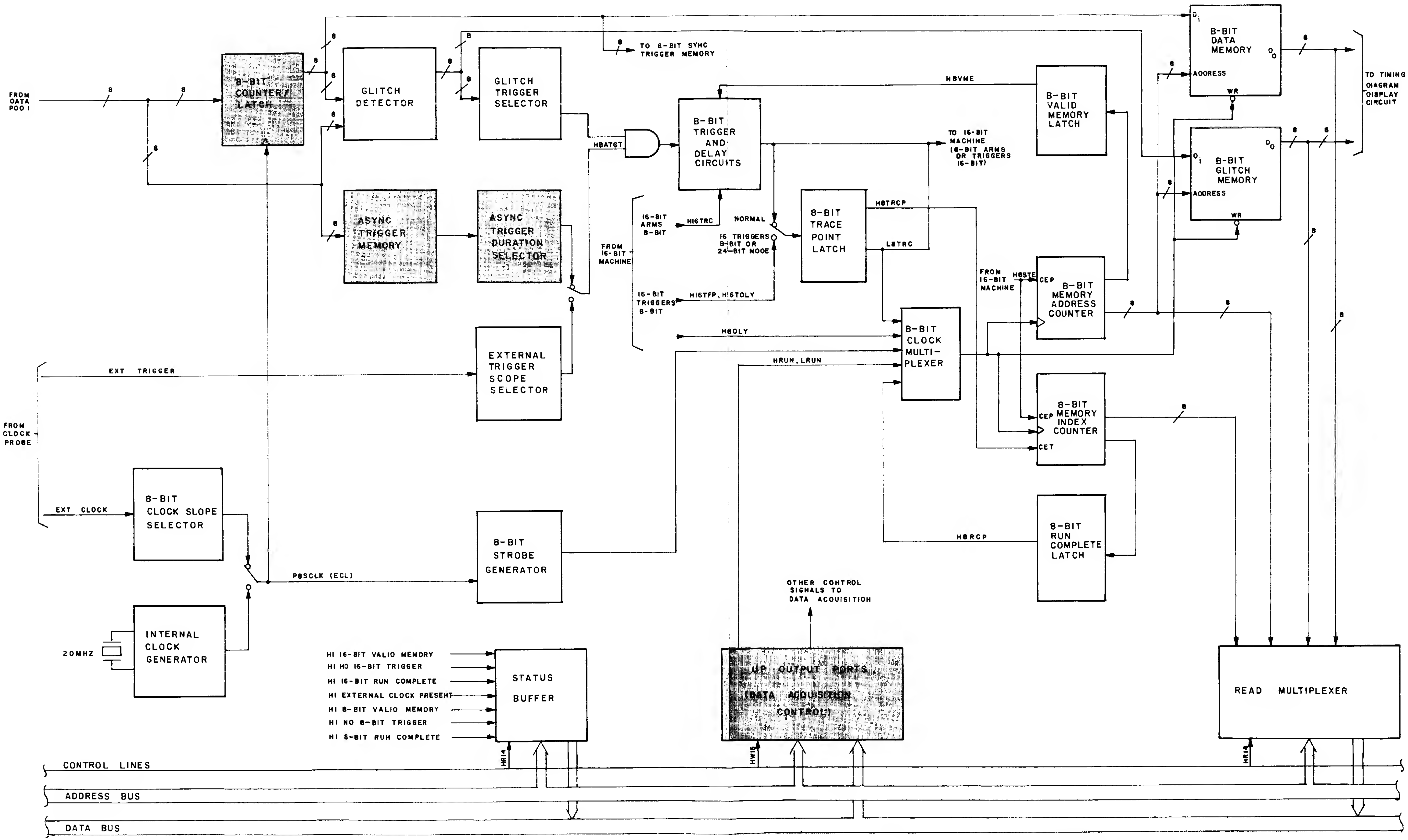


Figure 8-24. Block Diagram, 8-bit Data-acquisition Section for Schematic 5A

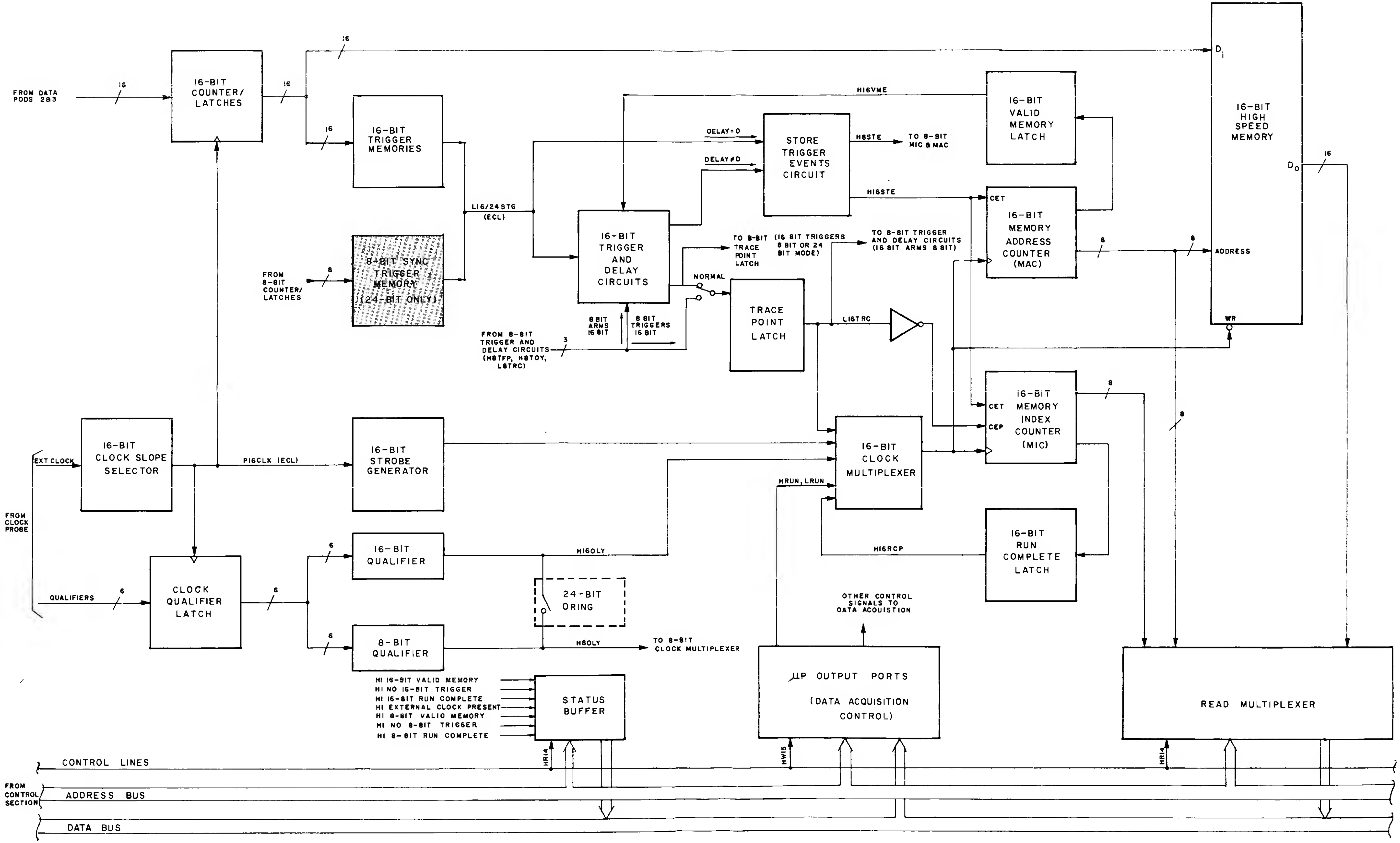


Figure 8-25.
Block Diagram, 16-bit Data-acquisition Section for Schematic 5A

SERVICE SHEET 5A

PRINCIPLES OF OPERATION

Trigger Memory Programming. There are two trigger memories on assembly A4: U2 and U3. Both trigger memories are loaded with the same trigger data, but only one memory is used during any trace. U2 is used during 24-bit synchronous traces, and U3 is used during 8-bit asynchronous traces.

When loading the trigger data into the trigger memories, the parallel-enable inputs of input latches U31 and U17 are high. This forces the input latches to operate as hexadecimal count-up counters. Their reset inputs are set high during the 300-μsec LMRST period, and then low again so that their count begins at binary 0. Their count addresses both memories: U2 directly, and U3 through U18 and U32. The data for each memory address (valid or invalid trigger state) is supplied from the microprocessor on data bus line HDB0.

At the end of the trigger-programming period, LDACQ (ECL) (Low Data Acquire, ECL) from U45A switches low, forcing U31 and U17 to operate as latches for data from the line receivers. The latches supply their outputs to the synchronous trigger memory and to translators U33 and U20 which drive the 8-bit sampled-data memory. The low also switches U18 and U32 to select the outputs from the line receivers and deliver these to the asynchronous trigger memory.

Synchronous Trigger Operation. The synchronous trigger memory (U2) is used during 24-bit synchronous operations. The software configures the machine to be in the 16-bit triggers 8-bit mode. L24BST(ECL) (Low 24-bit State, ECL) is low. It forces U45D low to enable U2. The output of U2 is wire ORed with the output from the 16-bit synchronous trigger memories on assembly A1. When the 24-bit trigger word is recognized, all outputs from the 16-bit trigger memories and the 8-bit synchronous trigger memory go low, providing L24BST(ECL). This provides for selecting trigger qualification on data sets up to 24 bits wide. In this mode, P8SCLK is the externally supplied synchronous trigger.

Asynchronous Trigger Operation. U3 is an ECL memory device. In the high output state, U3 can absorb high current, but in the low output state, U3 absorbs very little current. The input data through U18 and U32 is applied to the address inputs of U3. When these data comprise a valid trigger word, the output of U3 ramps down toward -5.2 V. When it crosses a preset threshold level, U1C generates a positive transition to initiate the 8-bit asynchronous trigger. If the trigger pattern occurs, but does not remain long enough for the U3 ramp to cross threshold, the high output from U3 will immediately reset the RC circuit to the high state.

The rate at which the low output state of U3 can change toward -5.2 V is dependent upon the trigger duration selected in the menu by the operator. With the fastest trigger duration selected, R6, adjustment R20, and C1 provide the shortest ramp-down period. Longer trigger durations are selected by providing a low output on one of the inverters in U19 via U46. This connects additional capacitance into the RC network. Each capacitor is dedicated to one of the trigger-duration selections.

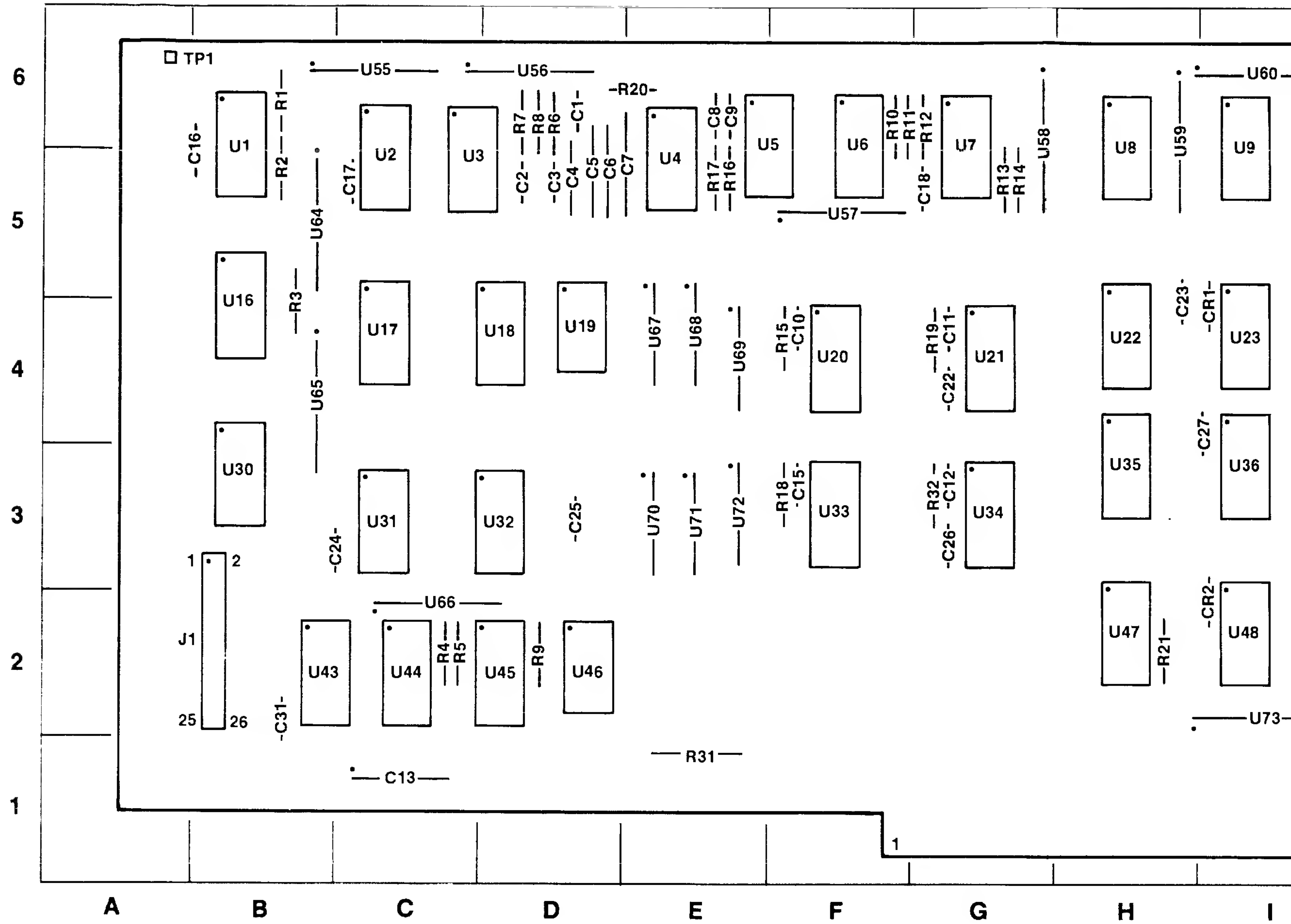
Trigger Generator. The asynchronous trigger generator consists of both sections of U43 and U44. LRST (Low Reset) switches low during microprocessor reset period to each trace. This ensures that the output of U43A is high and U43B is low. This sets U44B, providing the not-triggered output condition when the trace starts.

In 8-bit asynchronous triggering with no glitch trigger, U44B is used as an asynchronous latch. At the end of the reset period, LRST returns high again and remains high for the entire run. This enables one OR input to the AND functions of U43A and U43B. When U1C recognizes its trigger state for the selected duration, its positive transition satisfies the other OR inputs. Now U43A switches low and U43B switches high, resetting U44B to generate the 8-bit asynchronous trigger state. When the trigger state on U1C disappears, U43B switches low and U43A sets U44B again, ending the 8-bit asynchronous trigger state.

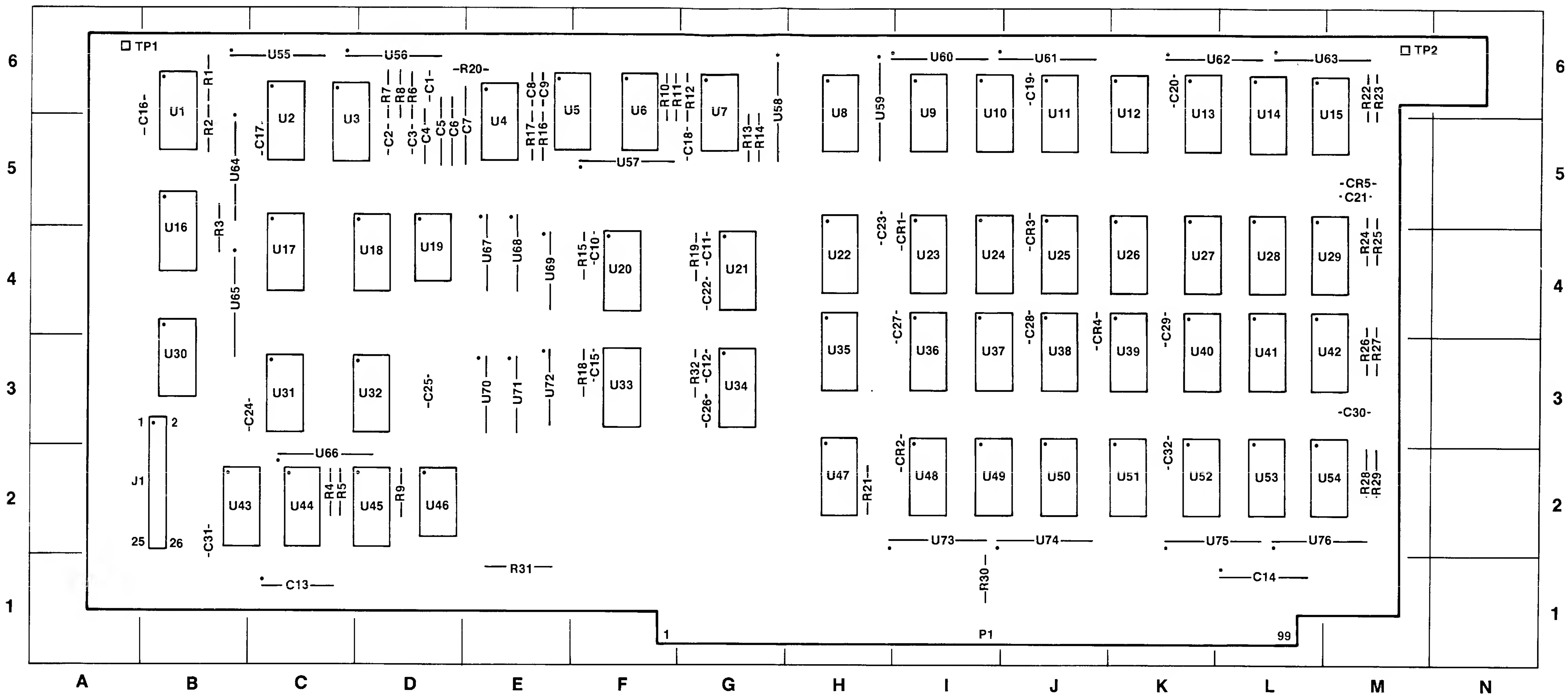
When glitch detection is included in the 8-bit asynchronous trace, U44A is added to the trigger circuitry and U43A is eliminated. The purpose of this change is to stretch the 8-bit asynchronous trigger state to ensure that glitches will be captured regardless of whether they occur within or outside of the normal sample period.

HGTRGENA (High Glitch Trigger Enable) is high in this mode. U6D uses this high state to satisfy one OR input of U43A. With LRST high, U43A will remain low. This releases the set input of U44B and the reset input of U44A. Now U44A remains in the set state and U44B in the reset state after the end of trigger recognition from U1C.

The D input of U44A is low after the end of the recognized trigger state from U1C. P8SCLK(ECL) (Positive 8-bit Sampled clock, ECL) clocks this low into U44A, resetting the $\overline{Q}$ output high. LGLITCHRESET(ECL) occurs after P8SCLK(ECL). It clocks the high on $\overline{Q}$ into U44B, ending the 8-bit asynchronous trigger condition.

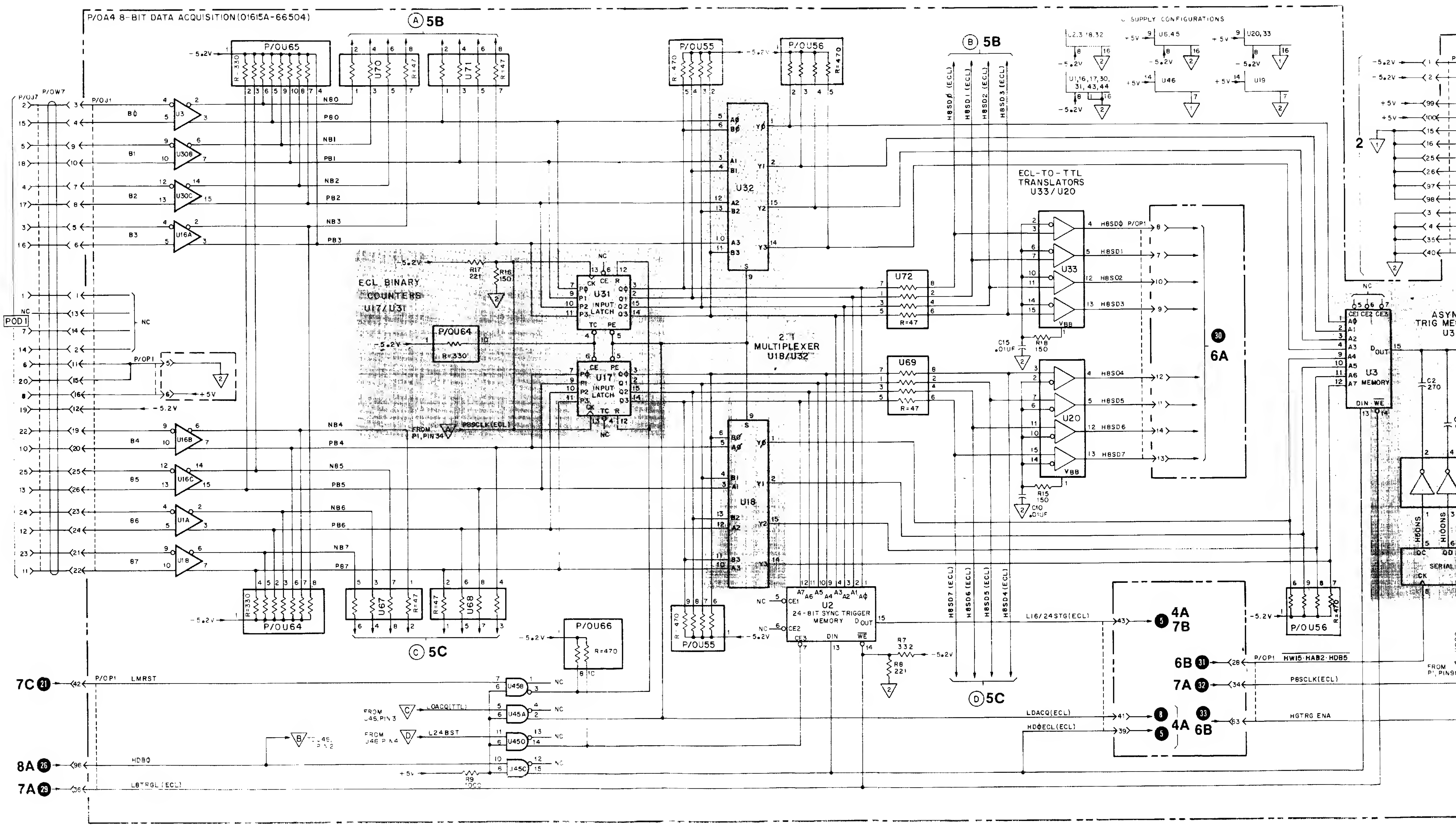


REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-6	C16	B-6	C31	B-2	R7	D-6	R22	M-6	U3	C-5	U18	D-4
C2	D-5	C17	C-5	C32	K-2	R8	D-6	R23	M-6	U4	E-5	U19	D-4
C3	D-5	C18	G-5	CR1	I-4	R9	D-2	R24	M-4	U5	E-6	U20	F-4
C4	D-5	C19	J-6	CR2	I-2	R10	F-6	R25	M-4	U6	F-6	U21	G-4
C5	D-5	C20	K-6	CR3	J-4	R11	F-6	R26	M-3	U7	G-6	U22	H-4
C6	D-5	C21	M-5	CR4	J-4	R12	G-6	R27	M-3	U8	H-6	U23	I-4
C7	E-5	C22	G-4	CR5	M-5	R13	G-5	R28	M-2	U9	I-6	U24	I-4
C8	E-6	C23	H-4	J-1	B-2	R14	G-5	R29	M-2	U10	I-6	U25	J-4
C9	E-6	C24	B-3	P1	I-1	R15	F-4	R30	I-1	U11	J-6	U26	K-4
C10	F-4	C25	D-3	R1	B-6	R16	E-5	R31	E-1	U12	K-6	U27	K-4
C11	G-4	C26	G-3	R2	B-5	R17	E-5	R32	G-3	U13	K-6	U28	L-4
C12	G-3	C27	I-4	R3	B-4	R18	F-3	TP1	A-6	U14	L-6	U29	M-4
C13	C-1	C2B	J-4	R4	C-2	R19	G-4	TP2	M-6	U15	M-6	U30	B-3
C14	L-1	C29	K-4	R5	C-2	R20	E-6	U1	B-6	U16	B-4	U31	C-3
C15	F-3	C30	M-3	R6	D-6	R21	H-2	U2	C-5	U17	C-4	U32	D-3



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-6	C16	B-6	C31	B-2	R7	D-6	R22	M-6	U3	C-5	U18	D-4	U33	F-3	U48	I-2	U63	M-6
C2	D-5	C17	C-5	C32	K-2	R8	D-6	R23	M-6	U4	E-5	U19	D-4	U34	G-3	U49	I-2	U64	B-5
C3	D-5	C18	G-5	CR1	I-4	R9	D-2	R24	M-4	U5	E-6	U20	F-4	U35	H-3	U50	J-2	U65	B-4
C4	D-5	C19	J-6	CR2	I-2	R10	F-6	R25	M-4	U6	F-6	U21	G-4	U36	I-3	U51	K-2	U66	C-2
C5	D-5	C20	K-6	CR3	J-4	R11	F-6	R26	M-3	U7	G-6	U22	H-4	U37	I-3	U52	K-2	U67	E-4
C6	D-5	C21	M-5	CR4	J-4	R12	G-6	R27	M-3	U8	H-6	U23	I-4	U38	J-3	U53	L-2	U68	E-4
C7	E-5	C22	G-4	CR5	M-5	R13	G-5	R28	M-2	U9	I-6	U24	I-4	U39	K-3	U54	M-2	U69	E-4
C8	E-6	C23	H-4	J-1	B-2	R14	G-5	R29	M-2	U10	I-6	U25	J-4	U40	K-3	U55	C-6	U70	E-3
C9	E-6	C24	B-3	P1	I-1	R15	F-4	R30	I-1	U11	J-6	U26	K-4	U41	L-3	U56	D-6	U71	E-3
C10	F-4	C25	D-3	R1	B-6	R16	E-5	R31	E-1	U12	K-6	U27	K-4	U42	M-3	U57	F-5	U72	E-3
C11	G-4	C26	G-3	R2	B-5	R17	E-5	R32	G-3	U13	K-6	U28	L-4	U43	B-2	U58	G-6	U73	I-2
C12	G-3	C27	I-4	R3	B-4	R18	F-3	TP1	A-6	U14	L-6	U29	M-4	U44	C-2	U59	H-6	U74	J-2
C13	C-1	C28	J-4	R4	C-2	R19	G-4	TP2	M-6	U15	M-6	U30	B-3	U45	D-2	U60	I-6	U75	K-2
C14	L-1	C29	K-4	R5	C-2	R20	E-6	U1	B-6	U16	B-4	U31	C-3	U46	D-2	U61	J-6	U76	L-2
C15	F-3	C30	M-3	R6	D-6	R21	H-2	U2	C-5	U17	C-4	U32	D-3	U47	H-2	U62	K-6		

Figure 8-26. Timing Data-acquisition Assembly A4. Parts Identification


P/OA4 8-BIT DATA ACQUISITION (01615A-66504)
ECL BINARY COUNTERS U17/U31
2:1 MULTIPLEXER U18/U32
ECL-TO-TTL TRANSLATORS U33/U20
24-BIT SYNC TRIGGER MEMORY
SUPPLY CONFIGURATIONS
POD 1
LMRST
HDB0
L8TRGL (ECL)
L16/24STG(ECL)
LDACQ(ECL)
HD0ECL(ECL)
P8SCLK(ECL)
HGTRG ENA

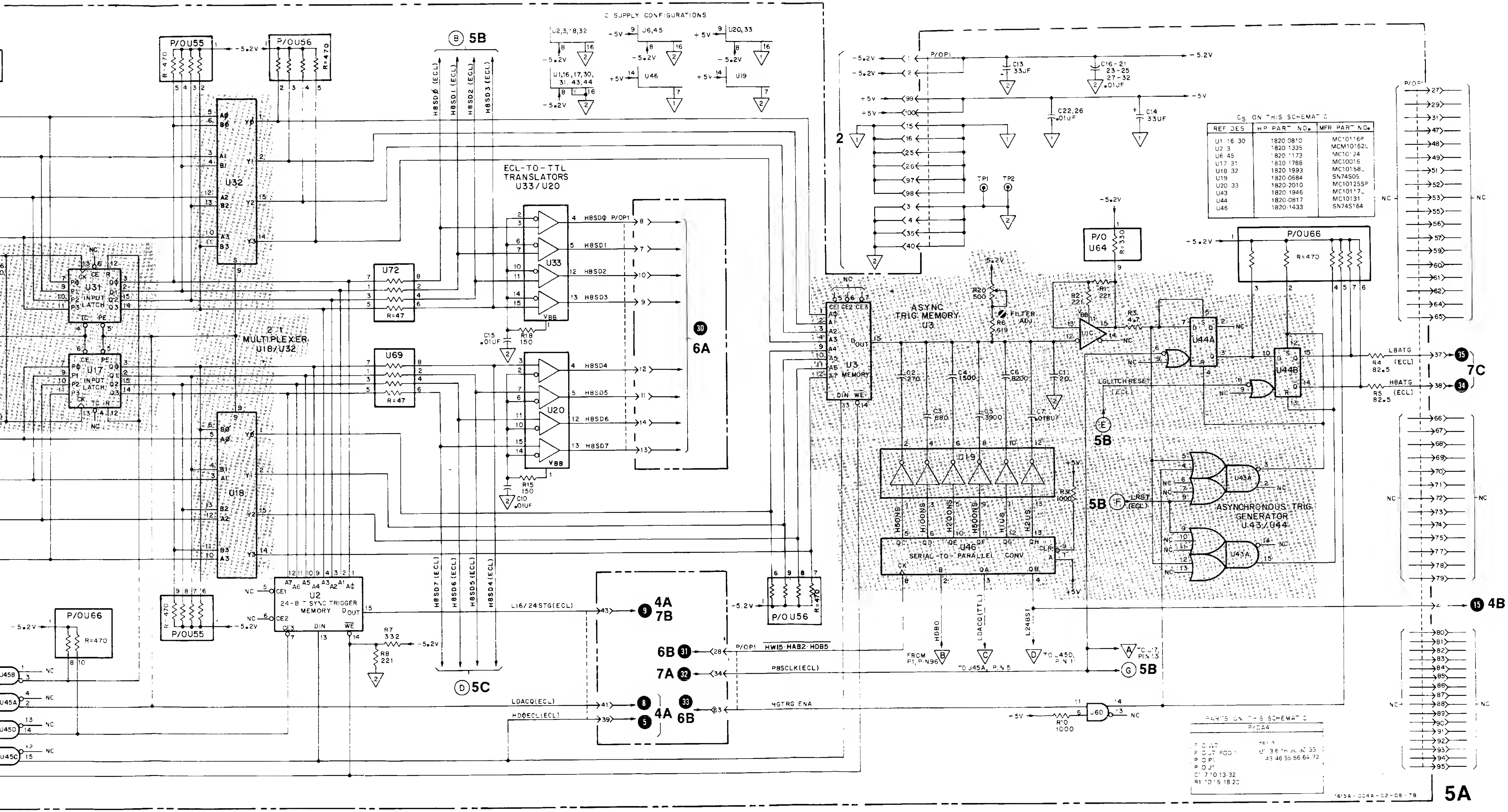


Figure 8-27. Timing Data-acquisition (P/O A4) Schematic

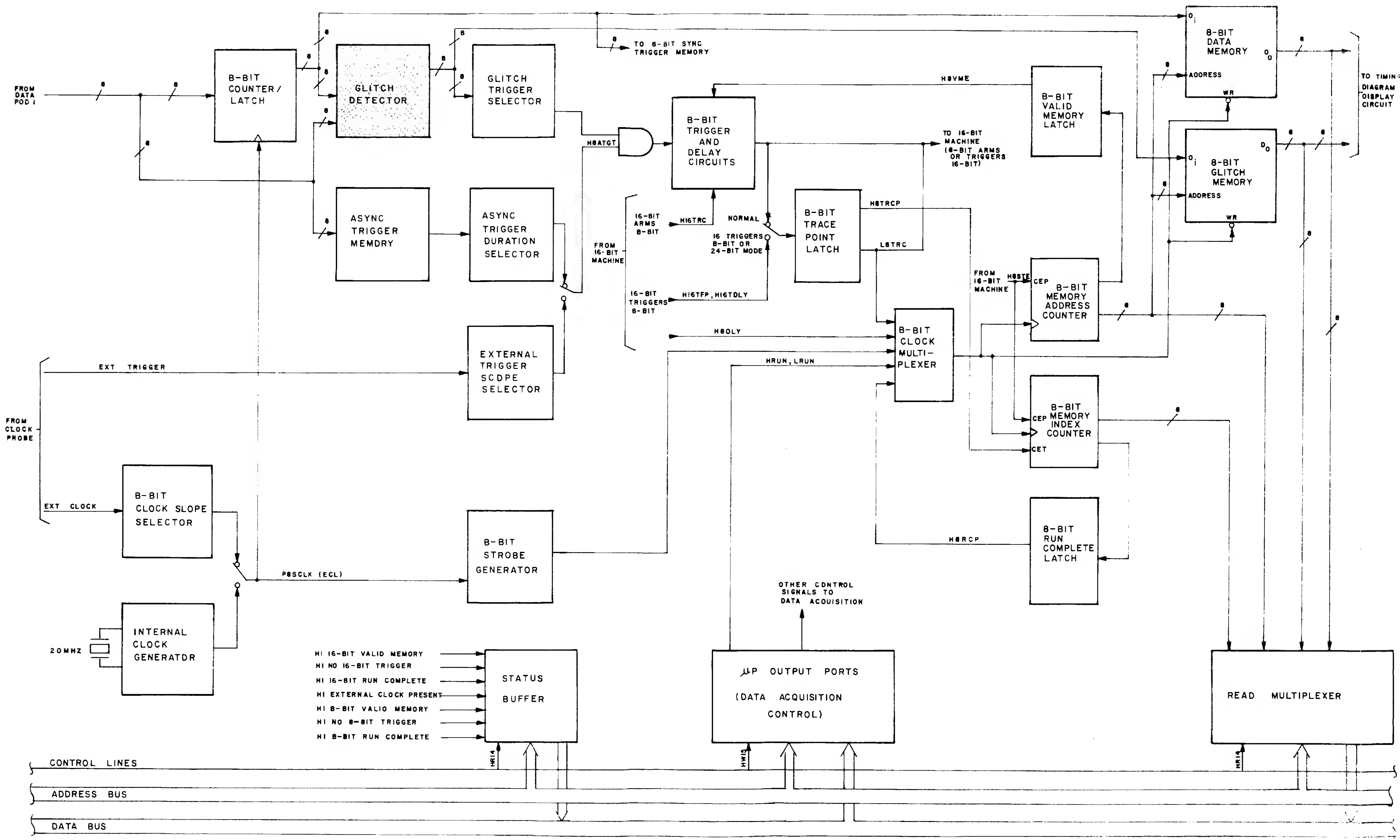


Figure 8-23. Block Diagram, 8-bit Data-acquisition Section for Schematic 5B

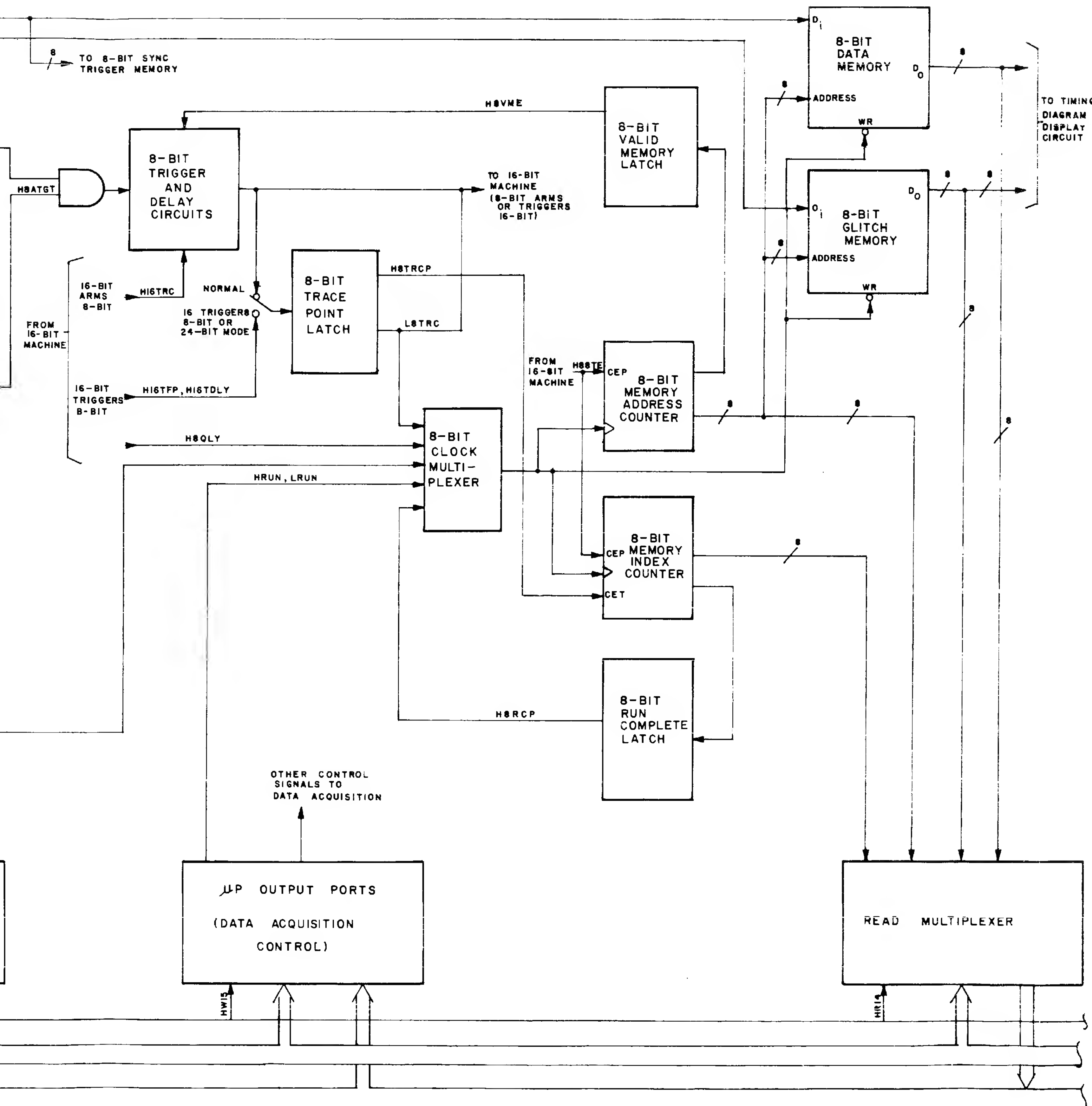
SERVICE SHEE

PRINCIPLES OF O

A glitch is defined a
directions within o
logic level at the be
plied as a reference
level of the channel
then a transition fr
sample period will

This discussion is
and accompanying
channels in probe p
All eight glitch dete
tor consists of two
detector halves op
One detector half
period. Then in the
cleared while the o

At T0, HRST (Hig
resets all four glit
start. At T1, P8SC
arrives. With each c
states, switching e
U7B/D. These OR
circuits when both
describe the case w
(U5B-Q is low and



ock Diagram, 8-bit Data-acquisition Section for Schematic 5B

SERVICE SHEET 5B

PRINCIPLES OF OPERATION

A glitch is defined as logic transitions occurring in both directions within one sample period. A sample of the logic level at the beginning of the sample period is supplied as a reference to each glitch detector. If the logic level of the channel is 0 at the start of the sample period, then a transition from logic 1 to logic 0 during that same sample period will indicate that a glitch has occurred.

This discussion is directed to the simplified schematic and accompanying set of waveforms. Each of the eight channels in probe pod 1 has a separate glitch detector. All eight glitch detectors are identical. Each glitch detector consists of two identical detector halves. The two detector halves operate on alternate sample periods. One detector half is active during the first sample period. Then in the next sample period, it is read and cleared while the other detector half is active.

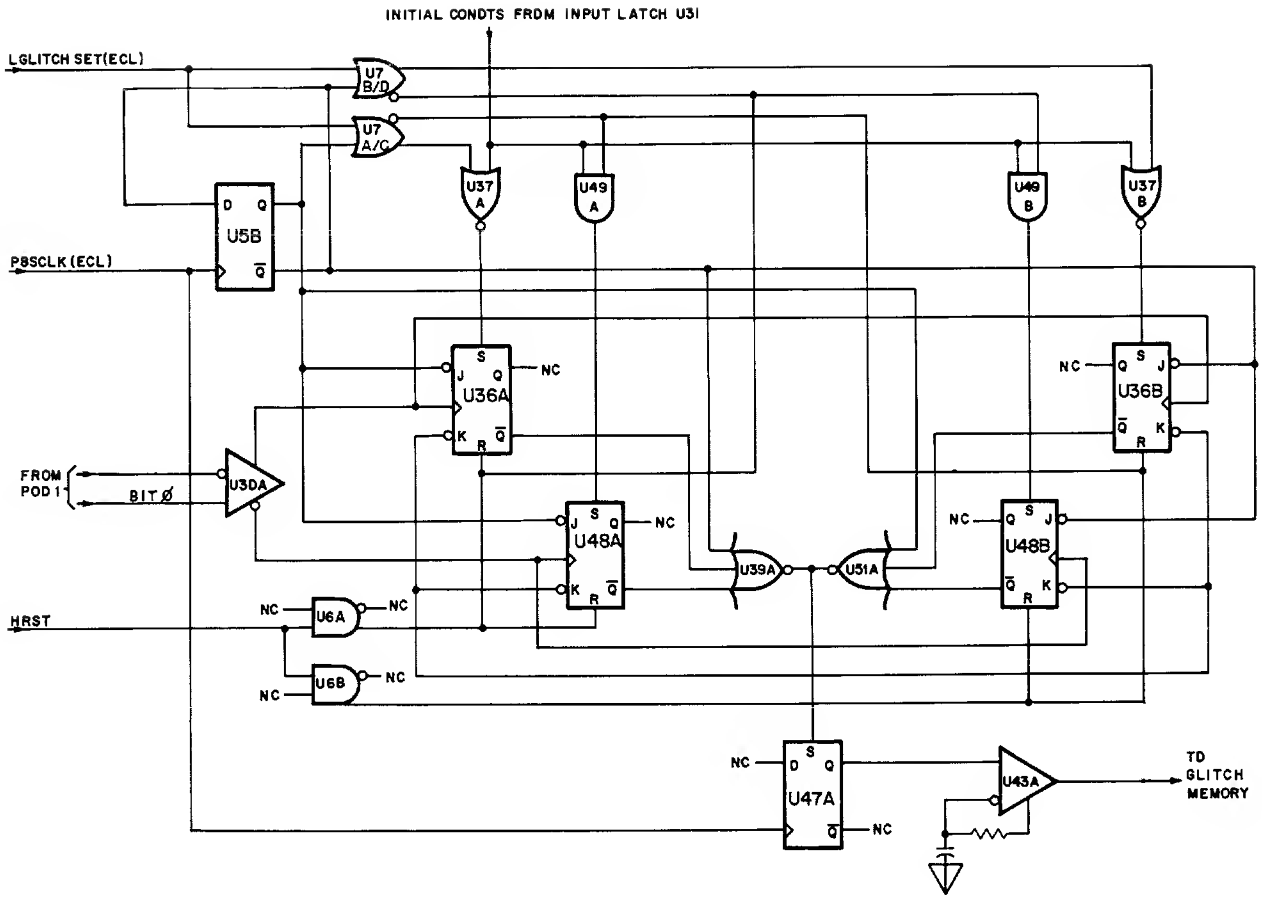
At T0, HRST (High Reset) from the microprocessor resets all four glitch-detection flip-flops prior to run start. At T1, P8SCLK(ECL) (8-bit Sample Clock, ECL) arrives. With each cycle of P8SCLK(ECL), U5B changes states, switching enable levels between U7A/C and U7B/D. These OR/NOR gates enable their associated circuits when both inputs are low. This discussion will describe the case where the enable is applied to U7A/C (U5B-Q is low and $\overline{Q}$ is high).

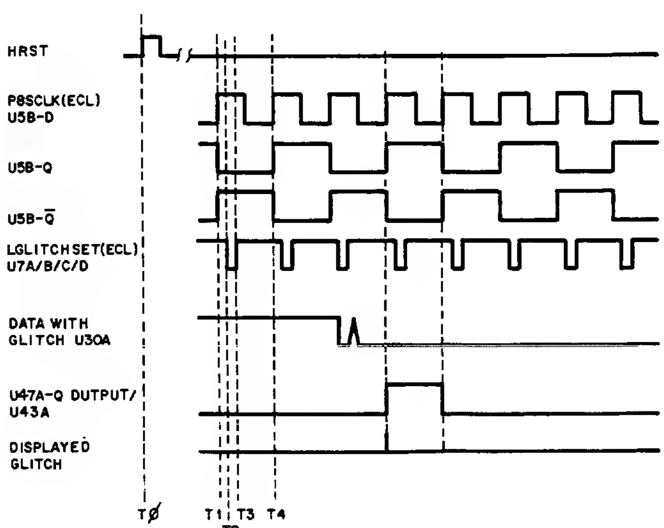
Since LGLITCHSET(ECL) is high at T1, no enable occurs in U7A/C, but enable levels are applied to the J inputs of glitch-detection flip-flops U36A and U48A. Any time that the line receiver detects a logic transition during the sample period, the associated glitch-detection flip-flop will clock its J input. A positive-going transition clocks one flip-flop and a negative-going transition is inverted to clock the other flip-flop.

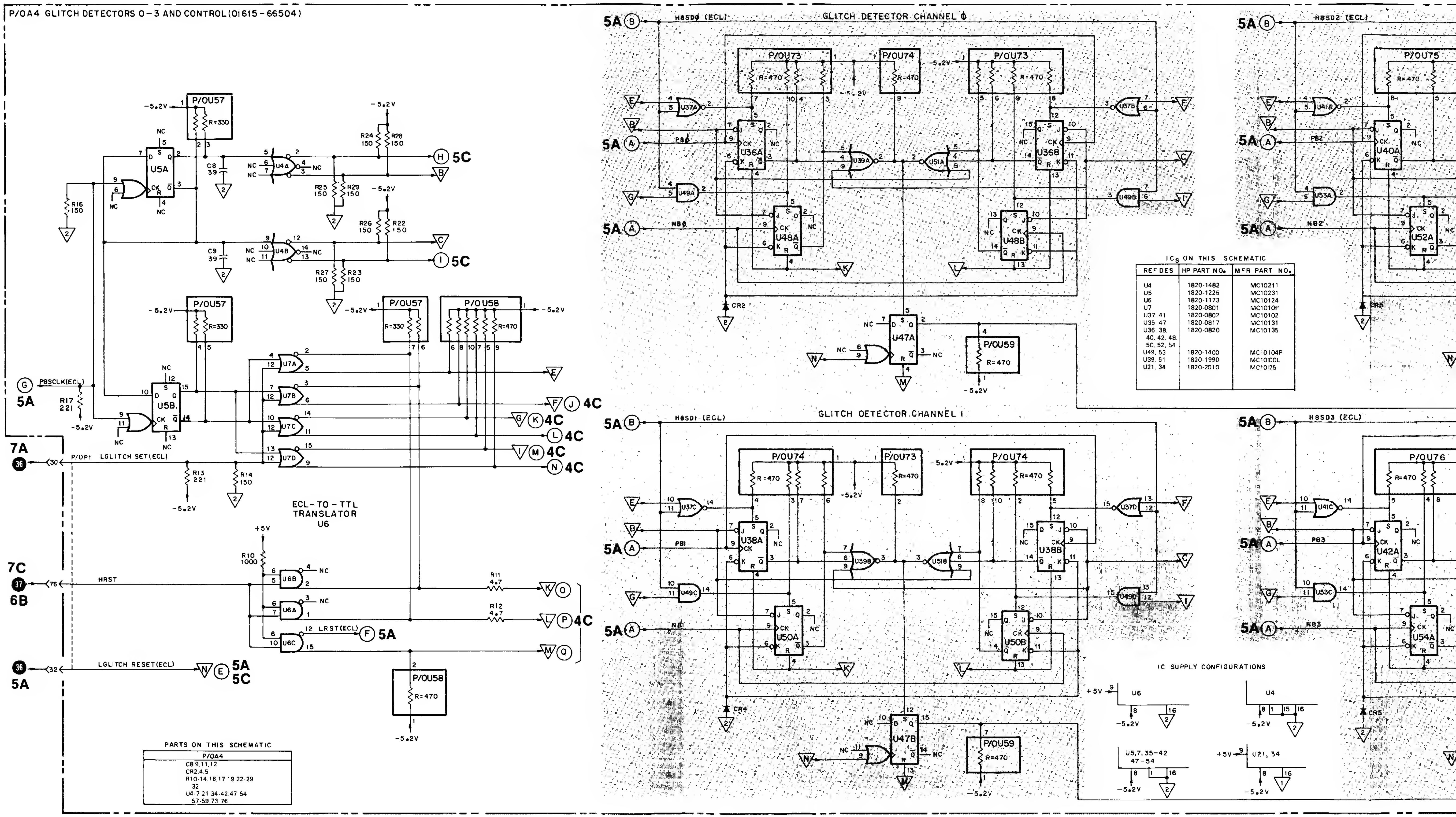
At T2, LGLITCHSET(ECL) switches low. This switches U7A/C to activate both initial-condition gates U37A and U49A. Depending upon the logic state of the initial condition, one of these two gates will set its associated flip-flop. The set flip-flop corresponds to a logic transition away from initial condition. The set flip-flop places logic 0 on the associated input of U39A.

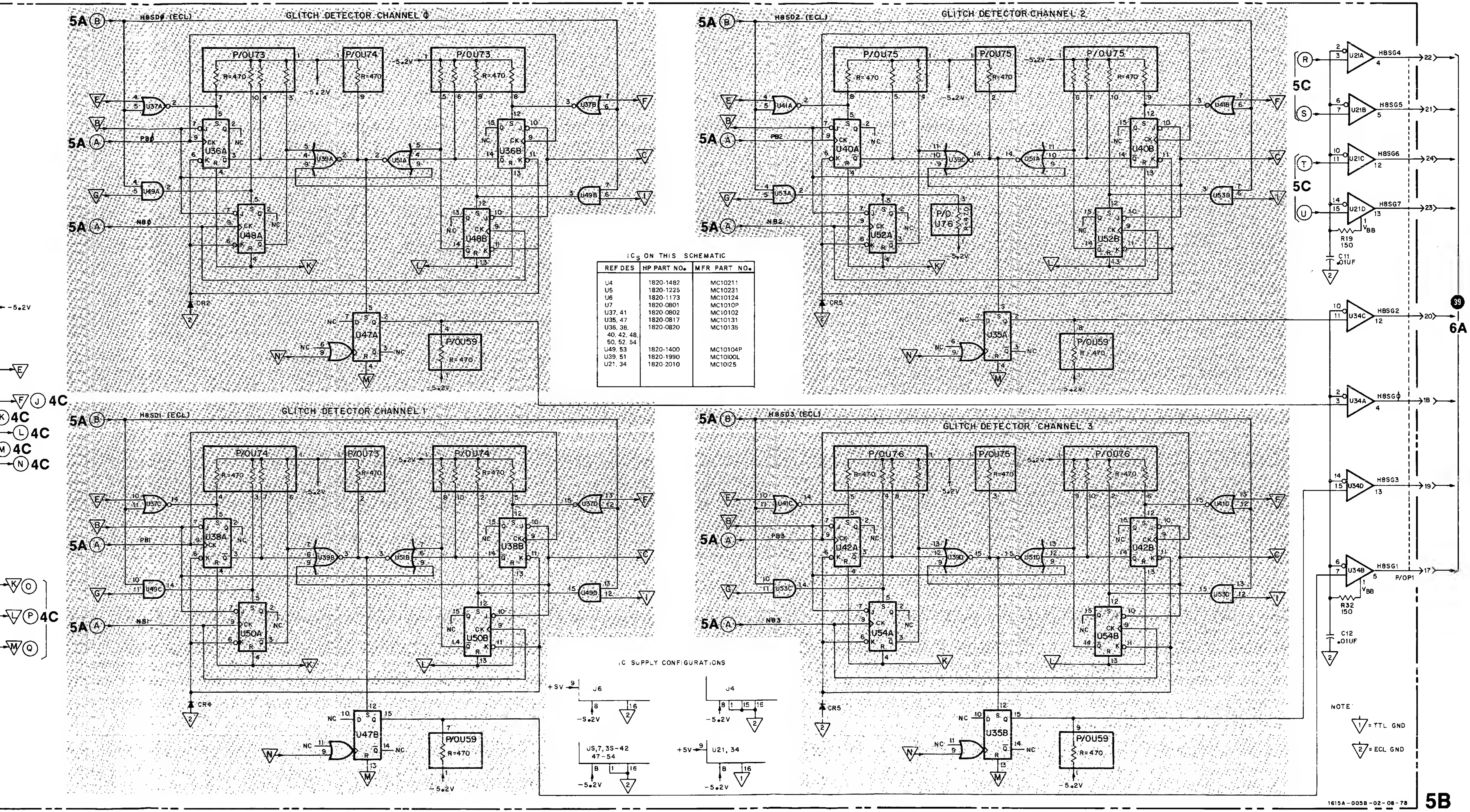
At T3, the initial-condition gates are disabled for the remainder of the sample period. Now the remaining JK flip-flop waits for its transition (transition to initial condition) to clock its logic 0 to U39A.

At T4, the outputs of U5B switch, removing the enable levels from the J inputs of U36A and U48A, and applying enable levels to the J inputs of the glitch-detection flip-flops in the other half of the circuit. Also, U5B applies logic 0 to the third input of U39A. If a glitch was detected during the sample period, both $\overline{Q}$ outputs from the flip-flops will be low. The third low now sets U39A high. This sets U47A high, providing the glitch-detected level through translator U43A to the glitch memory.


INITIAL CONDTS FROM INPUT LATCH U31
LGLITCH SET(ECL)
P8SCLK(ECL)
FROM POD 1
BIT Ø
HRST
U7 B/D
U7 A/C
U37 A
U49 A
U49 B
U37 B
U5B
U36A
U36B
U3DA
U48A
U48B
U39A
U51A
U6A
U6B
U47A
U43A
NC
TO GLITCH MEMORY


HRST
P8SCLK(ECL) U5B-D
U5B-Q
U5B-Q̄
LGLITCHSET(ECL) U7A/B/C/D
DATA WITH GLITCH U30A
U47A-Q OUTPUT/ U43A
DISPLAYED GLITCH
TØ
T1
T2
T3
T4


P/OA4 GLITCH DETECTORS 0-3 AND CONTROL (01615-66504)
GLITCH DETECTOR CHANNEL Ø
GLITCH DETECTOR CHANNEL 1
ECL-TO-TTL TRANSLATOR U6
P8SCLK(ECL)
P/OP1 LGLITCH SET(ECL)
HRST
LRST(ECL)
LGLITCH RESET(ECL)
H8SDØ (ECL)
H8SD1 (ECL)
H8SD2 (ECL)
H8SD3 (ECL)
IC SUPPLY CONFIGURATIONS
ICs ON THIS SCHEMATIC
REF DES | HP PART NO. | MFR PART NO.
U4 | 1820-1482 | MC10211
U5 | 1820-1225 | MC10231
U6 | 1820-1173 | MC10124
U7 | 1820-0801 | MC1010P
U37, 41 | 1820-0802 | MC10102
U35, 47 | 1820-0817 | MC10131
U36, 38, 40, 42, 48, 50, 52, 54 | 1820-0820 | MC10135
U49, 53 | 1820-1400 | MC10104P
U39, 51 | 1820-1990 | MC10100L
U21, 34 | 1820-2010 | MC10125
PARTS ON THIS SCHEMATIC
P/OA4
C8 9,11,12
CR2,4,5
R10-14,16,17 19 22-29 32
U4-7 21 34-42,47 54 57-59,73 76



ICS ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U4	1820-1482	MC10211
U5	1820-1225	MC10231
U6	1820-1173	MC10124
U7	1820-0801	MC1010P
U37, 41	1820-0802	MC10102
U35, 47	1820-0817	MC10131
U36, 38, 40, 42, 48, 50, 52, 54	1820-0820	MC10135
U49, 53	1820-1400	MC10104P
U39, 51	1820-1990	MC10100L
U21, 34	1820-2010	MC10125

Figure 8-29.
Glitch Detectors 0 through 3 and Control (P/O A4) Schematic

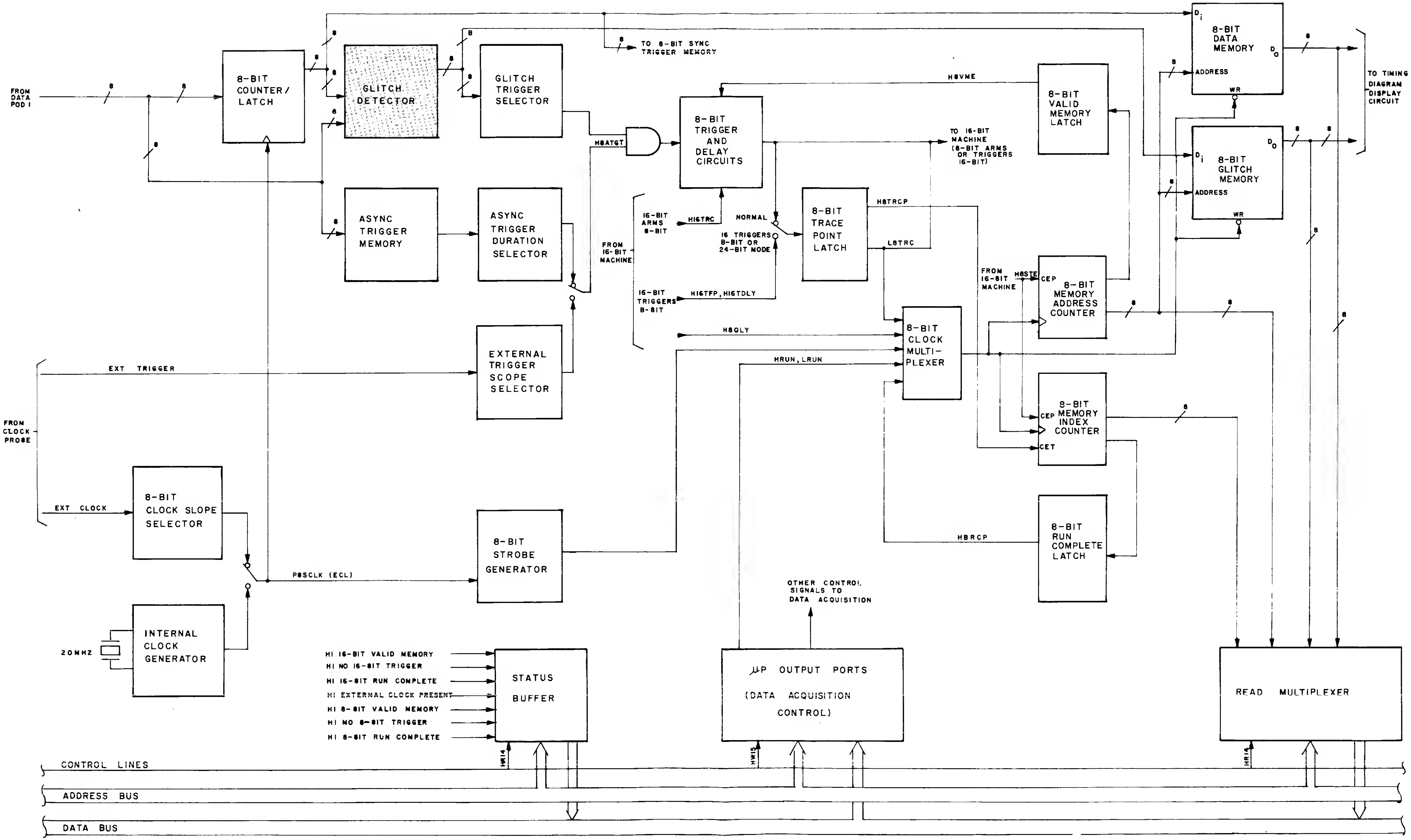
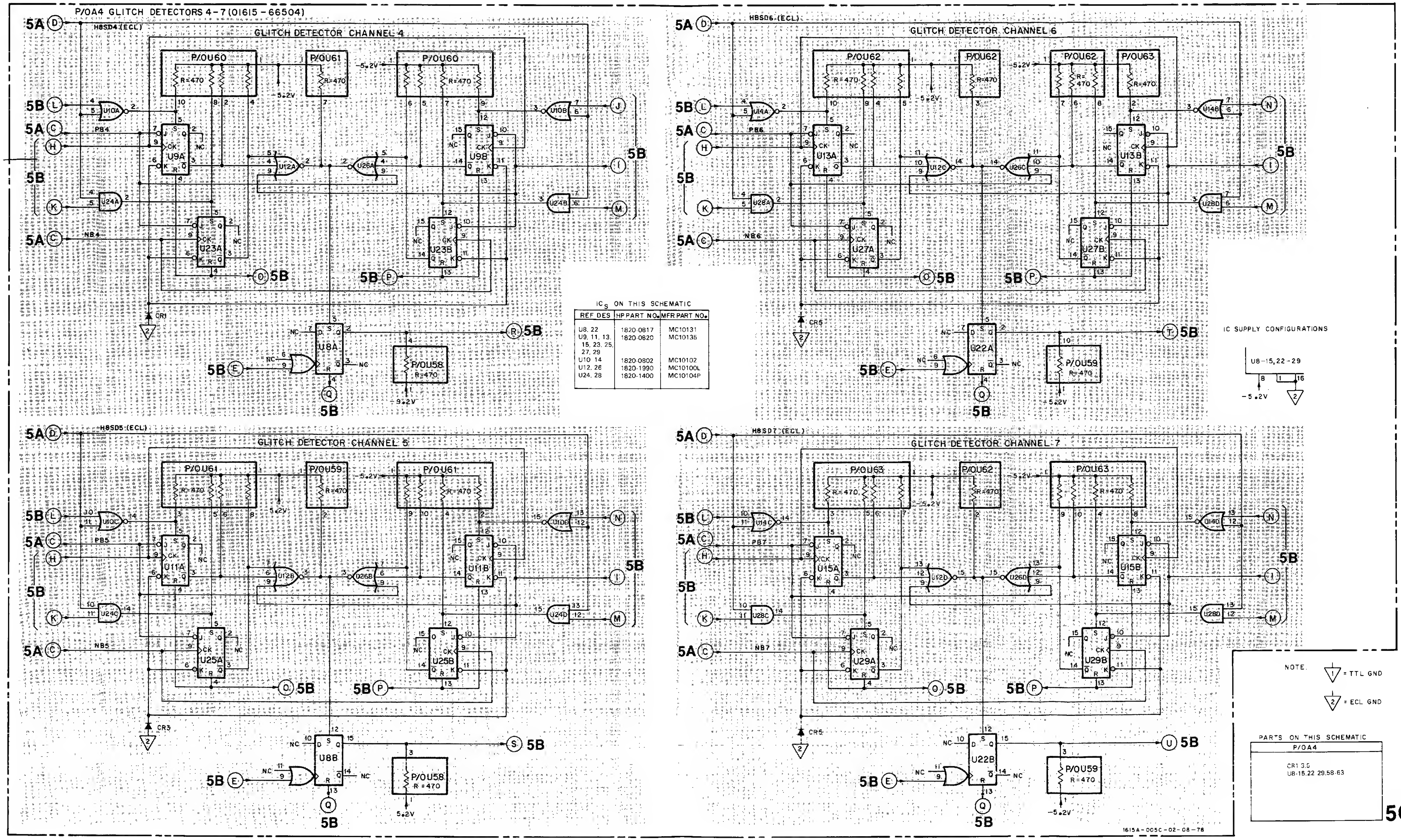


Figure 8-30. Block Diagram, 8-bit Data-acquisition Section for Schematic 5C



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U8, 22	1820-0817	MC10131
U9, 11, 13, 15, 23, 25, 27, 29	1820-0820	MC10135
U10 14	1820-0802	MC10102
U12, 26	1820-1990	MC10100L
U24, 28	1820-1400	MC10104P

PARTS ON THIS SCHEMATIC

P/OA4
CR1 3.5 U8-15.22 29.58-63

Figure 8-31.
Glitch Detectors 4 through 7 (P/O A4) Schematic

SERVICE SHEET 6A

PRINCIPLES OF OPERATION

Service sheet 4C contains a detailed explanation of the memories, output selectors, and counters used in the 16-bit synchronous data portion of the 1615A. Most of the explanation applies directly to the circuits shown on service sheet 6A for the 8-bit machine. Read the principles of operation given on service sheet 4C. The following paragraphs will discuss the differences between that circuitry and the circuitry used in the 8-bit machine.

Memory Index Counter. The purpose of the memory index counter is to end data capture when a full memory of valid data is obtained. There are three different modes of operation which use the memory index counter: START display with internal clock, START display with external clock, and END display with internal clock. (In the END display mode with external clock, the run stops when the trigger is recognized so the memory index counter is not used.)

Timing diagrams display 249 bits of memory along each trace on the CRT. Since the memory contains 256 locations, but displays only 249, 7 bits of captured data are blanked during display of a timing diagram. In order to position the trigger word within the 249 displayed bits, the memory index counter is preloaded to a different count for each of the three modes. The particular value of preload in each mode is governed by the logic levels of H8START (High 8-bit Start Display) and H8ECLK (High 8-bit External Clock). The preload occurs when LMRST (Low Master Reset) switches low before each new run.

START Display/External Clock. In this mode, the memory index counter is preloaded to binary 1 (pin 3 of U37 high and all other U37 and U38 inputs low). With this preload, the trigger word will be stored in memory location 0. The first 249 bits of captured data are displayed in this mode.

START Display/Internal Clock. In this mode, the memory index counter is preloaded to binary 16. This places the trigger word in memory location 15. The first seven locations in memory are masked by the channel number. Then the next 249 memory locations are presented on the display. In this mode, 240 bits of data acquisition will be captured before the counter signals run complete. There will be 15 words in memory preceeding the trigger word; thus 8 bits of pretrigger information will be displayed.

END Display/Internal Clock. In this mode, the memory index counter is preloaded to binary 241. This ensures that 15 additional words of data will be captured in memory after trigger recognition; thus 8 bits of post-trigger information will be displayed.

The memory index counter will count to 255 and generate terminal count. The high terminal count is ANDed with H8STE (High 8-bit Store Trigger Events) in U23C, placing a high on the D input of U36B. H8STE is always high, except during receipt of a word other than the trigger word when in the trace events mode. The next clock (clock 256) will set U36B, providing H8RCP which stops the flow of clocks to the 8-bit memory.

Up/Down Counters U44 and U45. In the unmagnified mode of operation, these counters are used to remember the address of data 0 (the first word captured in memory during a trace). The memory address counter always stops at the address of data 0 when a trace is complete. At the end of each trace, the microprocessor parallel-enables U44 and U45 to assume this address.

In the unmagnified mode of operation, the first seven bits of display are used to present the channel number. The next 249 words of memory (beginning with data bit 8) are displayed as the timing diagram. At the end of each sweep, LMACLD (Low Memory Address Counter Load) switches low. This parallel-enables U31 and U32 to the address from the up/down counter before beginning the next sweep.

In START display with external clock, the trigger word is located in data 0. Normally this portion of the data memory is used to show the channel number. To obtain a display which shows data 0 as the first word in the timing diagram, the up/down counter is counted down seven addresses by the software when this mode is selected. Now it assumes the address of data bit 249. When the display begins, the memory address counter is parallel-enabled to address 249. The alphanumeric channel number is presented during the first seven bits of display, and timing diagram begins with the eighth bit to be counted, data 0.

Memory Index Counter and Associated Logic. To understand the function of the memory index counter and the associated logic used in the 8-bit circuitry, each of the four 8-bit modes of operation must be described.

Start Display with Internal Clock. In this mode, the trigger point is the eighth dot into the display. H8START is high on pin 4 of U5A. Each 14th count of the memory address counter is decoded by U18C which places a low on pin 5 of U5A. This places a high state on the J input of U19B. The 15th clock in the trace generates H8VME from U19B.

H8VME enables the trigger circuitry. After trigger requirements are met, the next occurrence of P8CCLK will clock the memory index counter. The memory index counter advances to count 255 and enables U36B. The next P8CCLK will generate H8RCP which stops clocks during data acquisition, leaving the memory address counter at the address of data 0. Since the trigger is located at state 15, it will appear as the eighth bit on the timing diagram display.

Start Display with External Clock. H8VME is valid from the moment this mode is selected. H8START places a high on pin 11 of U5B. H8ECLK places a high on pin 10. This forces U5B low, setting U19B to generate H8VME. In this mode, the memory index counter is parallel-enabled to binary 1 at the start of the trace. This places the trigger word in data 0 of the memory index counter. Since H8RCP is generated at count 255 of the memory index counter plus one clock for U36B, the memory address counter is stopped at data 0, the trigger word.

End Display with Internal Clock. In this mode, H8VME is generated at count 255 of the memory address counter plus one clock for U19B. H8START is low, placing a high state on pin 3 of U5A. Terminal count in the memory address counter is inverted by U21D to place a low on pin 2 of U5A. This places a high state on the J input of U19B. The next clock to U19B generates H8VME, enabling the trigger circuitry. When trace point is recognized, pin 6 of U36 (schematic 6B) goes high, permitting the memory index counter to respond to incoming clocks. The memory index counter is parallel-enabled to count 241 at the beginning of a trace. This places the trace point at data 240 of the memory index counter. H8RCP is generated at count 255 plus one clock for U36B. This permits the 1615A to end the trace. Since the trace point is located in data 240, the trigger point is nine clocks in from the end of the timing diagram on the display.

End Display with External Clock. In this mode, the memory index counter is not used. U46A decodes this mode and sets U36B high to provide H8RCP immediately. H8START is low, placing a high state on pin 3 of U5A. Pin 2 switches low at terminal count from the memory address counter. This places a high state on the J input of U19B. The next clock generates H8VME. This releases the data-acquisition circuitry to search for the trigger that will end data-acquisition.

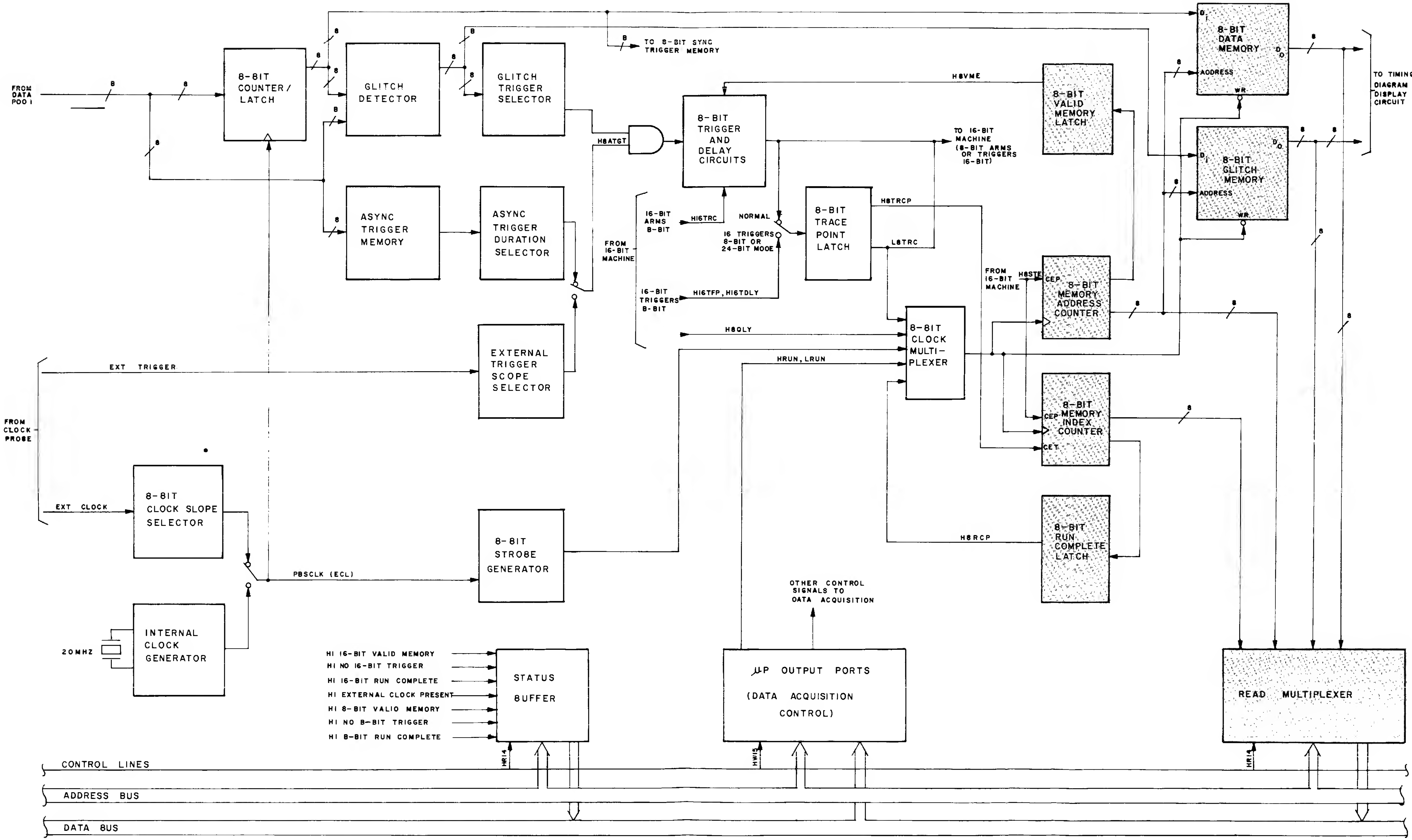


Figure 8-32.
Block Diagram, 8-bit Data-acquisition Section for Schematic 6A

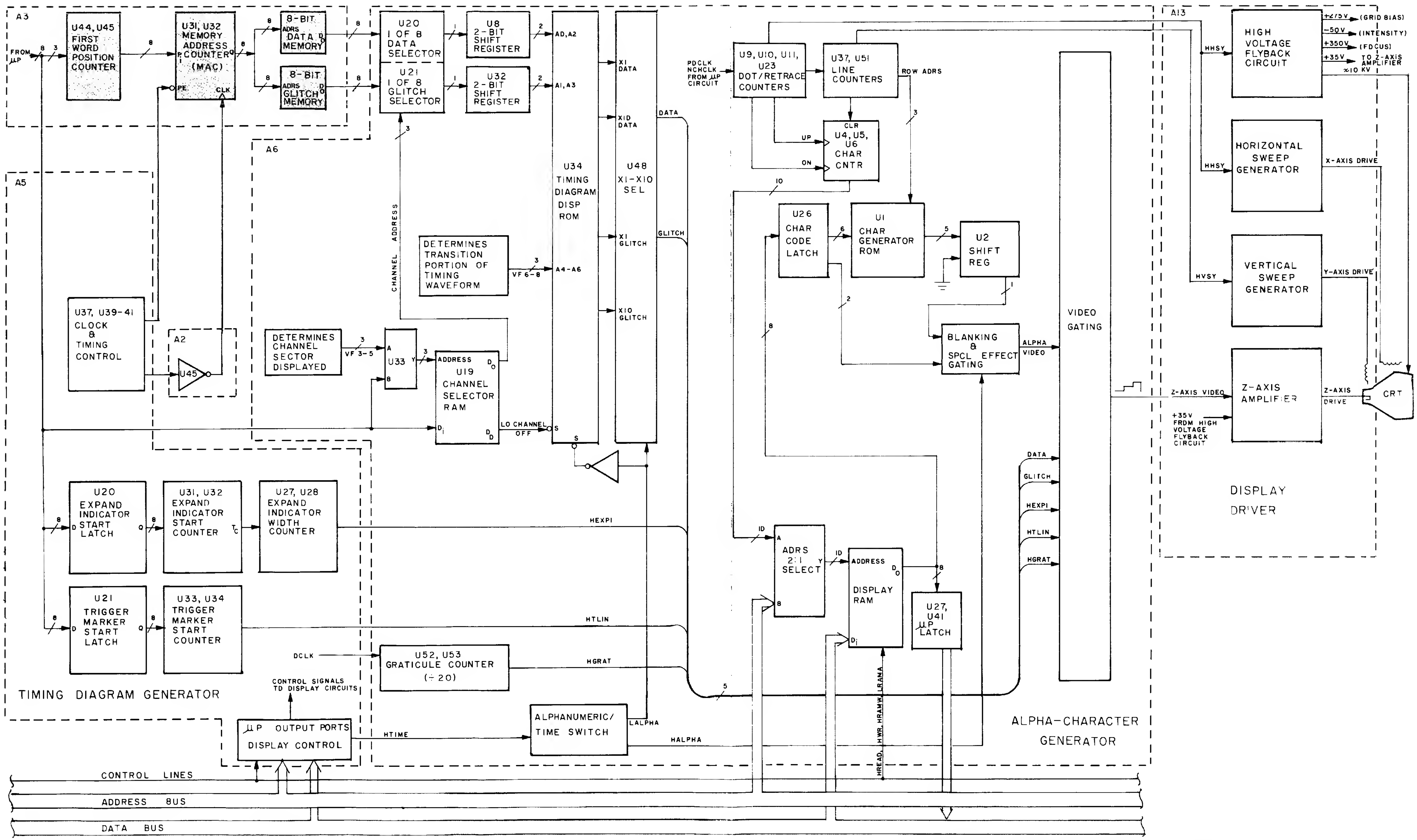


Figure 8-33. Block Diagram, Display Section for Schematic 6A

SIGNATURE ANALYSIS FOR SCHEMATIC 6A.

The signatures on this schematic are obtained by using DSA Setups A, C, and D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A3 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A3, and install A3 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ↓
STOP .... ↑
CLOCK .... ↓

Signatures for DSA Setup A (Schematic 6A)

Pin	Signature	Pin	Signature
VH A3U1-16	C690	A3U48-9	427H
A3U20-5	FHPA	A3U49-7	C43H
A3U20-6	7C7A	A3U49-9	C6P3
A3U44-1	57CA	A3U50-7	08F5
A3U44-9	7C7A	A3U50-9	AHA3
A3U45-1	57CA	A3U51-7	FHPA
A3U45-9	7C7A	A3U51-9	57CA
A3U48-7	FA2P		

DSA SETUP C.

1. Remove assembly A3 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A3 and install A3 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   d. Connect signature analyzer stop line to same point as start line, step c above.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 part number is 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ↑
STOP .... ↑
CLOCK .... ↓

Signatures for DSA Setup C (Schematic 6A)

Pin	Signature	Pin	Signature
VH A3U1-16	0001	A3U49-14	UUUU
A3U35-9	0AFA	A3U49-15	59UA
A3U46-11	59UA	A3U50-1	59UA
A3U46-12	3827	A3U50-2	5555
A3U46-13	0AFA	A3U50-14	UUUU
A3U48-1	59UA	A3U50-15	59UA
A3U48-2	5555	A3U51-1	59UA
A3U48-14	UUUU	A3U51-2	5555
A3U48-15	59UA	A3U51-14	UUUU
A3U49-1	59UA	A3U51-15	59UA
A3U49-2	5555		

DSA SETUP D.

1. Remove assembly A3 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A3 and install A3 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   c. Connect signature analyzer stop line to same point as start line, step b above.

   d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{\text{WR}}$ line.

4. Reinstall A5 in 1615A mainframe.

NOTE

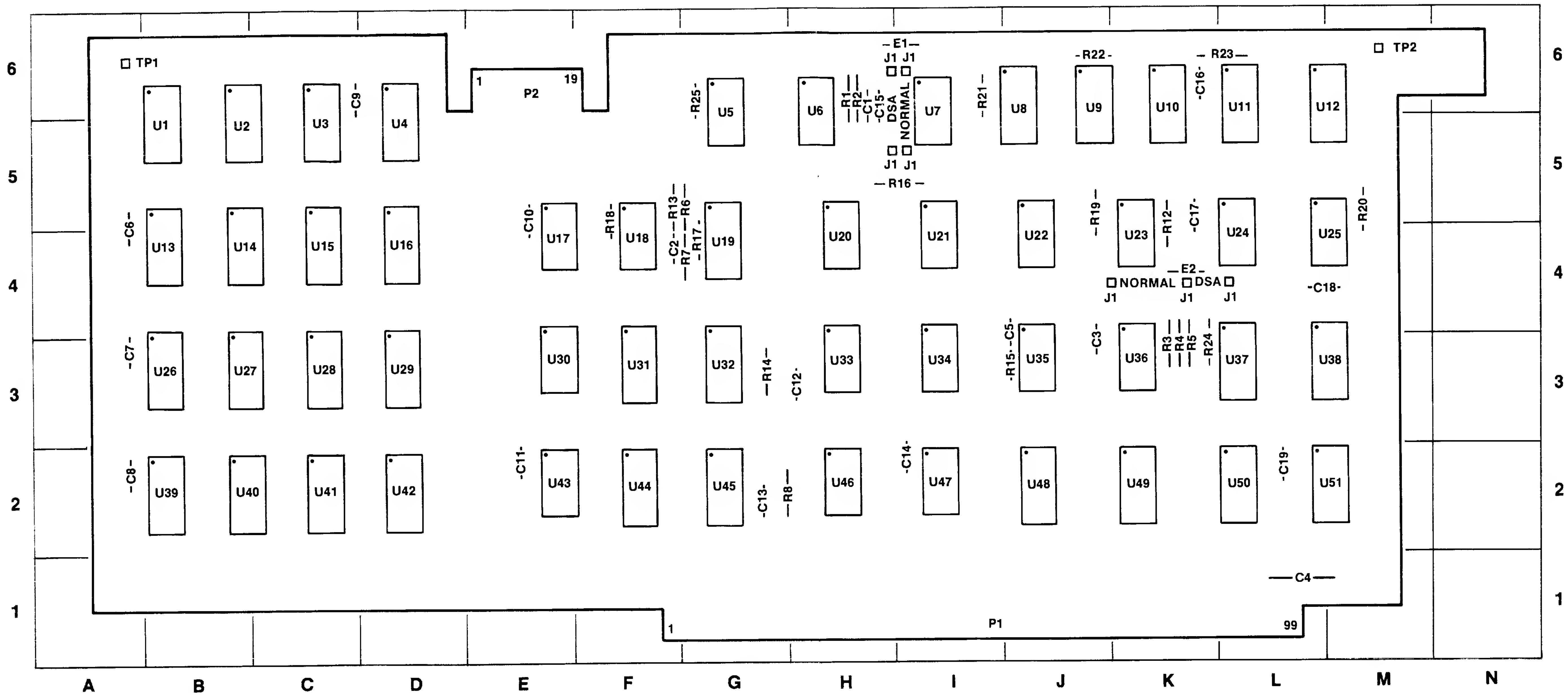
DSA jumper on A5 remains in NM (normal) position for this test setup.

5. Set up signature analyzer as follows:

START .... ↑
STOP .... ↑
CLOCK .... ↑

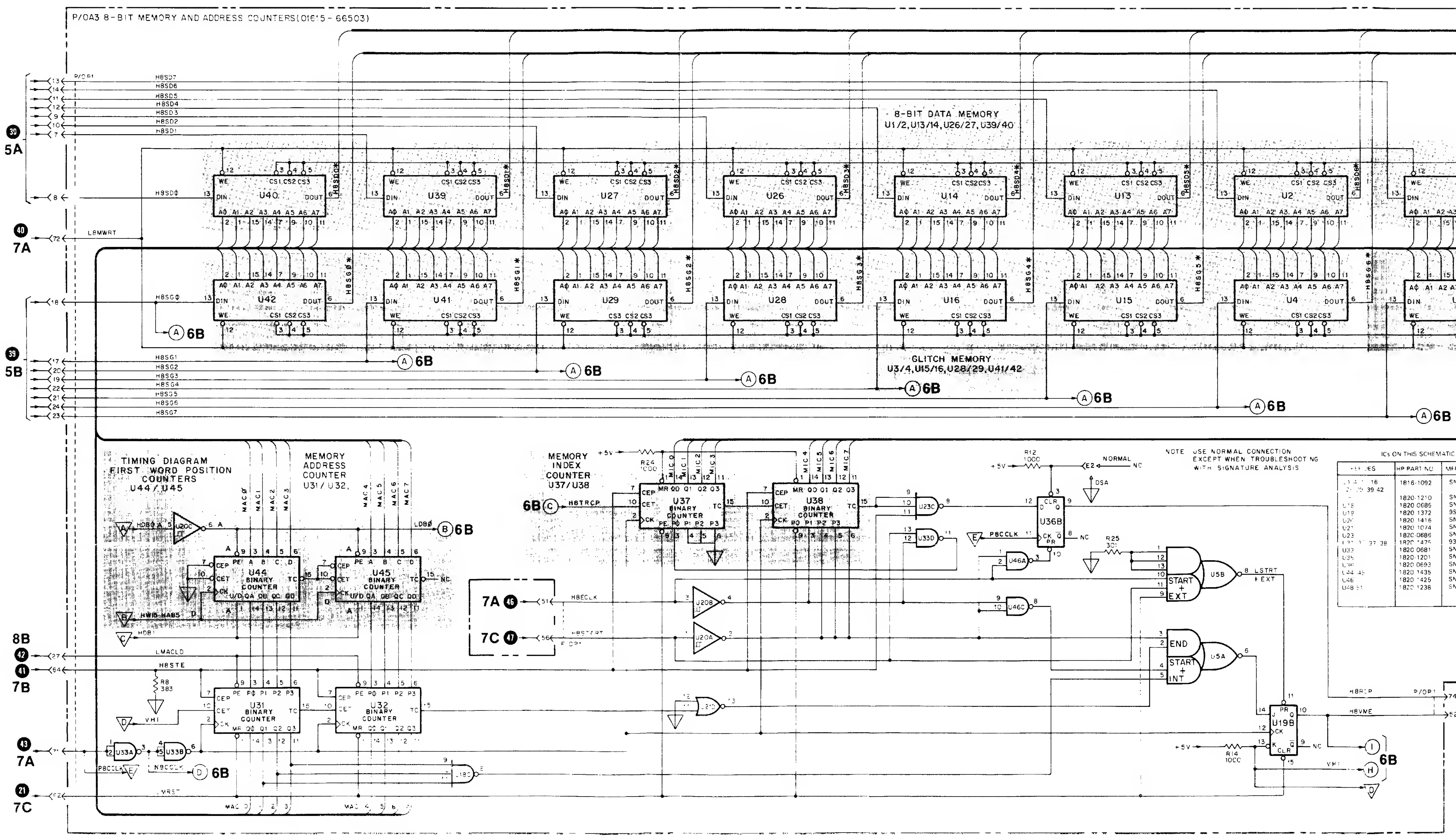
Signatures for DSA Setup D (Schematic 6A)

Pin	Signature	Pin	Signature
VH A3U1-16	0001	A3U44-2	H59F
A3U35-8	H59F	A3U45-2	H59F
A3U35-9	0AFC	A3U46-13	0AFC
A3U35-10	755P		



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	H-6	C15	H-6	R6	G-5	R23	L-6	U10	K-6	U24	L-4	U38	M-3
C2	F-4	C16	K-6	R7	G-4	R24	K-3	U11	L-6	U25	M-4	U39	8-2
C3	J-3	C17	K-5	R8	G-2	R25	G-6	U12	M-6	U26	8-3	U40	8-2
C4	L-1	C18	M-4	R12	K-5	TP1	A-6	U13	B-4	U27	B-3	U41	C-2
C5	J-4	C19	L-2	R13	F-5	TP2	M-6	U14	B-4	U28	C-3	U42	D-2
C6	A-5	E1	I-6	R14	G-3	U1	B-5	U15	C-5	U29	D-3	U43	E-2
C7	A-3	E2	K-4	R15	J-3	U2	B-5	U16	D-4	U30	E-3	U44	F-2
C8	A-2	P1	I-1	R16	I-5	U3	C-6	U17	E-4	U31	F-3	U45	G-2
C9	C-6	P2	E-6	R17	G-4	U4	D-5	U18	F-4	U32	G-3	U46	H-2
C10	E-5	R1	H-6	R18	F-5	U5	G-6	U19	G-4	U33	H-3	U47	I-2
C11	E-2	R2	H-6	R19	J-5	U6	H-6	U20	H-4	U34	I-3	U48	J-2
C12	H-3	R3	K-3	R20	M-5	U7	I-6	U21	I-4	U35	J-3	U49	K-2
C13	G-2	R4	K-3	R21	I-6	U8	J-6	U22	J-4	U36	K-3	U50	L-2
C14	I-2	R5	K-3	R22	J-6	U9	J-6	U23	K-4	U37	L-3	U51	M-2

Figure 8-34. Memory Assembly A3. Parts Identification



P/OA3 8-BIT MEMORY AND ADDRESS COUNTERS(01615-66503)
8-BIT DATA MEMORY
U1/2, U13/14, U26/27, U39/40
GLITCH MEMORY
U3/4, U15/16, U28/29, U41/42
TIMING DIAGRAM
FIRST WORD POSITION
COUNTERS
U44/U45
MEMORY
ADDRESS
COUNTER
U31/U32
MEMORY
INDEX
COUNTER
U37/U38
NOTE USE NORMAL CONNECTION EXCEPT WHEN TROUBLESHOOTING WITH SIGNATURE ANALYSIS
ICs ON THIS SCHEMATIC
5A
7A
5B
8B
7B
7A
7C
6B

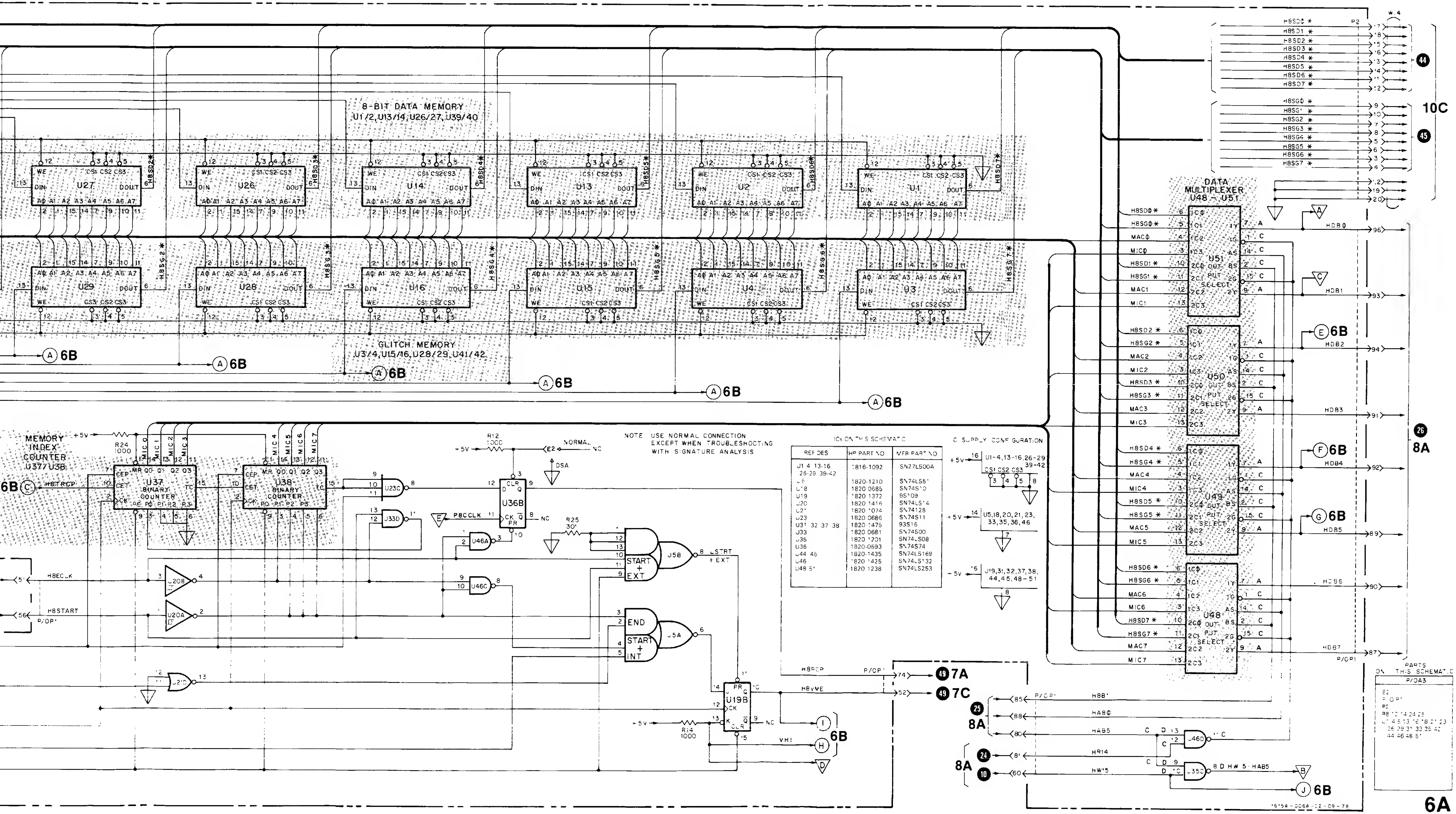


Figure 8-35.
Timing Memory and Address Counters (P/O A3) Schematic

SERVICE SHEET 6B

PRINCIPLES OF OPERATION

Trigger Mode and Delay. Prior to run start, the microprocessor clocks logic levels from $\overline{HDB0}$ into U22, U24, and U25. These logic levels select the delay count and mode of triggering for the 8-bit machine, according to the menu selections made by the 1615A operator. The delay count is parallel-enabled into the 8-bit delay counter (U8 through U12) before trigger recognition. When trigger recognition occurs H8TFP switches high from U19A, releasing the delay counter to respond to P8TCLK (Positive 8-bit Trigger Clock).

Glitch Trigger. When a glitch requirement is selected as part of the trigger specification, pin 5 of U22 is set high. U17 is loaded with high logic levels to activate each channel that will be monitored for a glitch. Each high level activates one AND gate in U43 or U30. The channels which are not selected receive low levels from U17. If a glitch in channel 0 is selected as part of the trigger specification, U17 places a high state on pin 10 of U43 and low states on all other pins of U43 and U30. When a glitch is detected in channel 0, H8SG0 will switch high, completing the AND requirement for U43. This forces U43 low which produces a high state from U18B. This activates one side of U6D to accept H8ATGT (8-bit Asynchronous Trigger).

The menu shows the glitch requirement as an OR field. One channel in U43 or U30 is enabled for each glitch trigger specified. Any glitch detected in any one of the enabled channels will satisfy the requirements of U18D. When no glitch is required as part of the trigger specification, U22 sets pin 3 of U18D low, enabling U6D.

Asynchronous Trigger. H8ATGT occurs during the time that the 8-bit trigger is recognized. U21B and U21C supply the 8-bit trigger to a connector on the 1615A rear panel for triggering an oscilloscope. When loading trigger information into the trigger memories, HLDTG prevents U21C from generating triggers to the rear-panel connector.

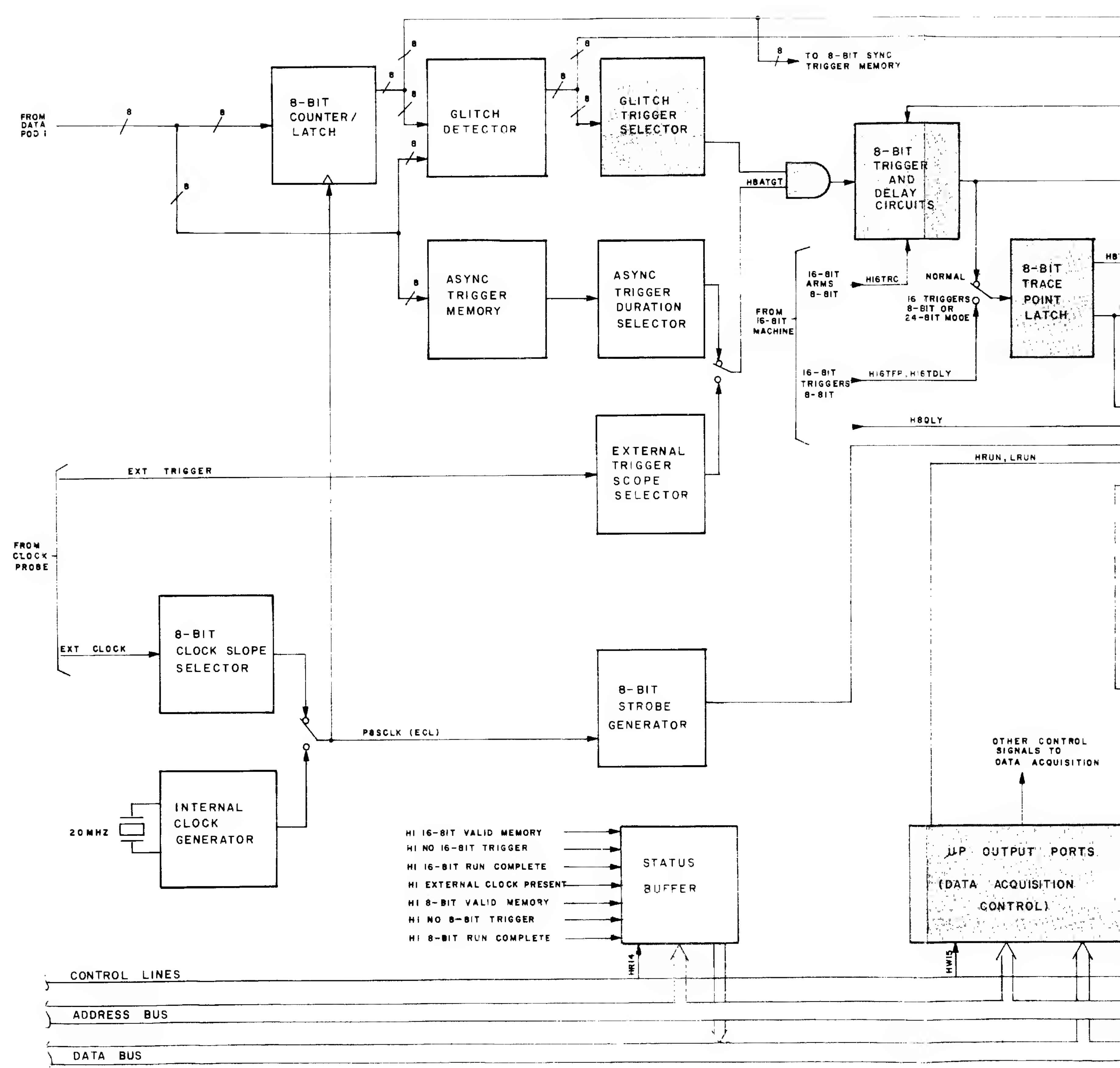
When H8ATGT occurs, U6D switches low, depending upon glitch requirements. This low sets RS latch U6A and U6B. With the RS latch set, the next clock will generate H8TFP (High 8-bit Trigger Flip-flop) from the Q output of U19A. H8TFP is supplied to U47, pin 5. If no trigger delay was selected, U47 will generate L8TRC (Low 8-bit Trace Point).

If a delay was specified, pin 6 of U47 will control generation of L8TRC. U23A decodes states 14 and 15 from U8. This is ANDed with H8TFP and terminal count from delay counter U12. U23B generates a high state one clock period before the end of the delay period selected in the menu. This high state is placed on the D inputs of U34A and U34B. U34A activates U47 to generate L8TRC, and U34B initiates the reset function.

U33 inverts L8TRC and applies a high state to pin 3 of U47. Pin 2 of U47 is always high, except during HRST (High Reset) before each trace. This latching circuit ensures that once L8TRC switches low, it will remain low for the entire trace. U36A synchronizes the internal clock with the external clock to control count-enable in the memory index counter.

Reset Logic. U34B supplies a high state to U7B when the trigger plus delay specification is met. The other input to the AND function in U7B is H8TFP. When U7B switches low, it clears U34B and initiates a high reset pulse from U6C to clear U7A and U7B. This resets RS latch U6A and U6B and trigger flip-flop U19A.

24-bit Mode. In 24-bit synchronous operation, the 1615A captures synchronous data words up to 24 bits wide. To do this, the 1615A triggers in the 16-bit triggers 8-bit mode. H16TRG8 is high on pins 1 and 13 of U47. When both the 8-bit and 16-bit trigger memories meet their specified trigger words, assembly A2 supplies H16TFP. H16TDLY is ANDed with the first two signals at the end of the selected delay period. This generates L8TRC from U47. Since L8TRC is coincident with L16TRC in this mode, both machines acquire data at the same point.



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n 5. If no
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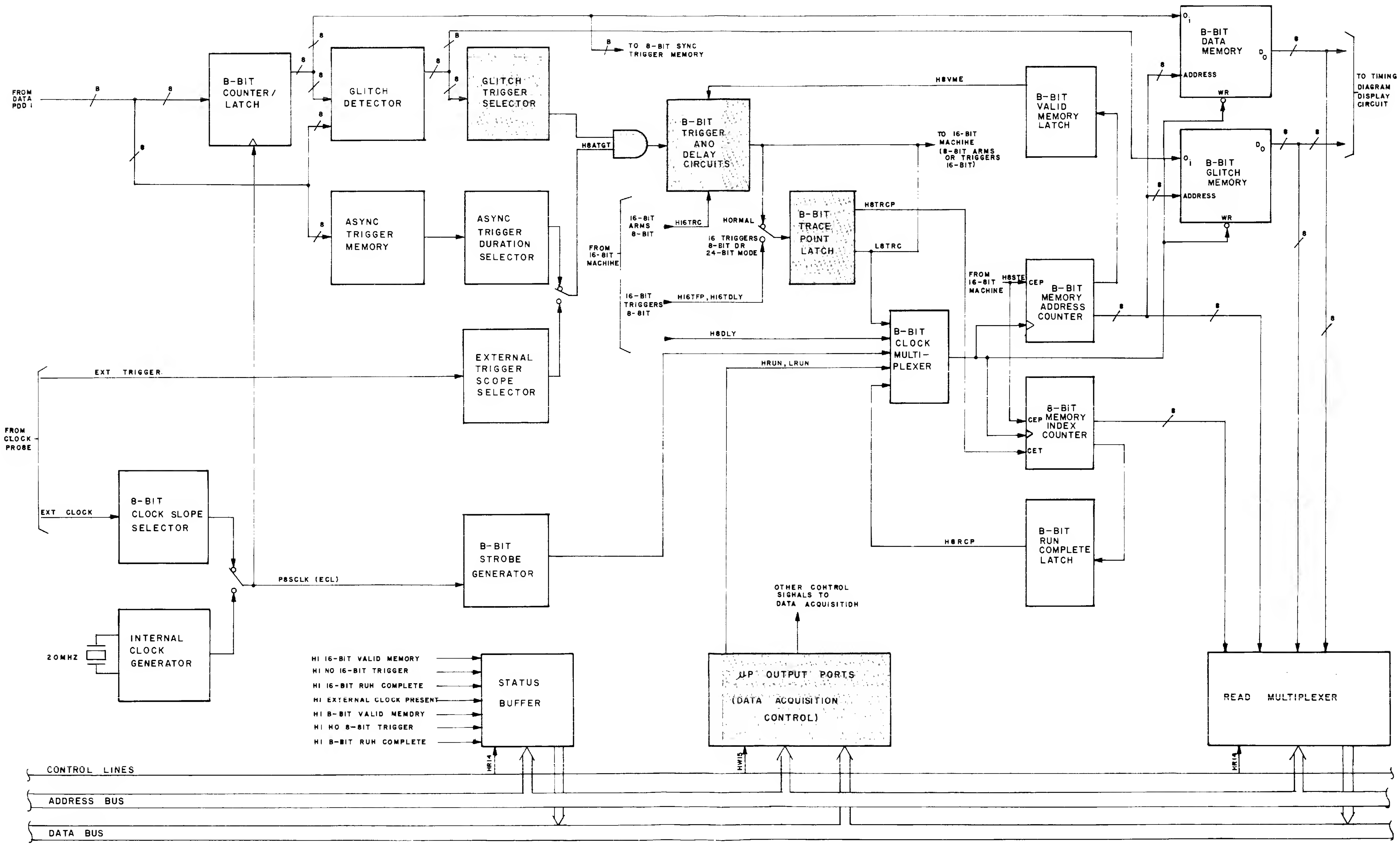


Figure 8-36. Block Diagram, 8-bit Data-acquisition Section for Schematic 6B

SIGNATURE ANALYSIS FOR SCHEMATIC 6B.

The signatures on this schematic are obtained by using DSA Setups A and D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A3 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A3, and install A3 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in the 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ↓
STOP.................................... ↑
CLOCK.................................. ↓

Signatures for DSA Setup A (Schematic 6B)

Pin	Signature
VH A3U1-16	C690
A3U17-2	7C7A
A3U22-2	7C7A
A3U35-1	08F5
A3U35-13	C43H
A3U46-5	C6P3

DSA SETUP D.

1. Remove assembly A3 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A3 and install A3 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   c. Connect signature analyzer stop line to same point as start line, step b above.

   d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{WR}$ line.

4. Reinstall A5 in 1615A mainframe.

NOTE

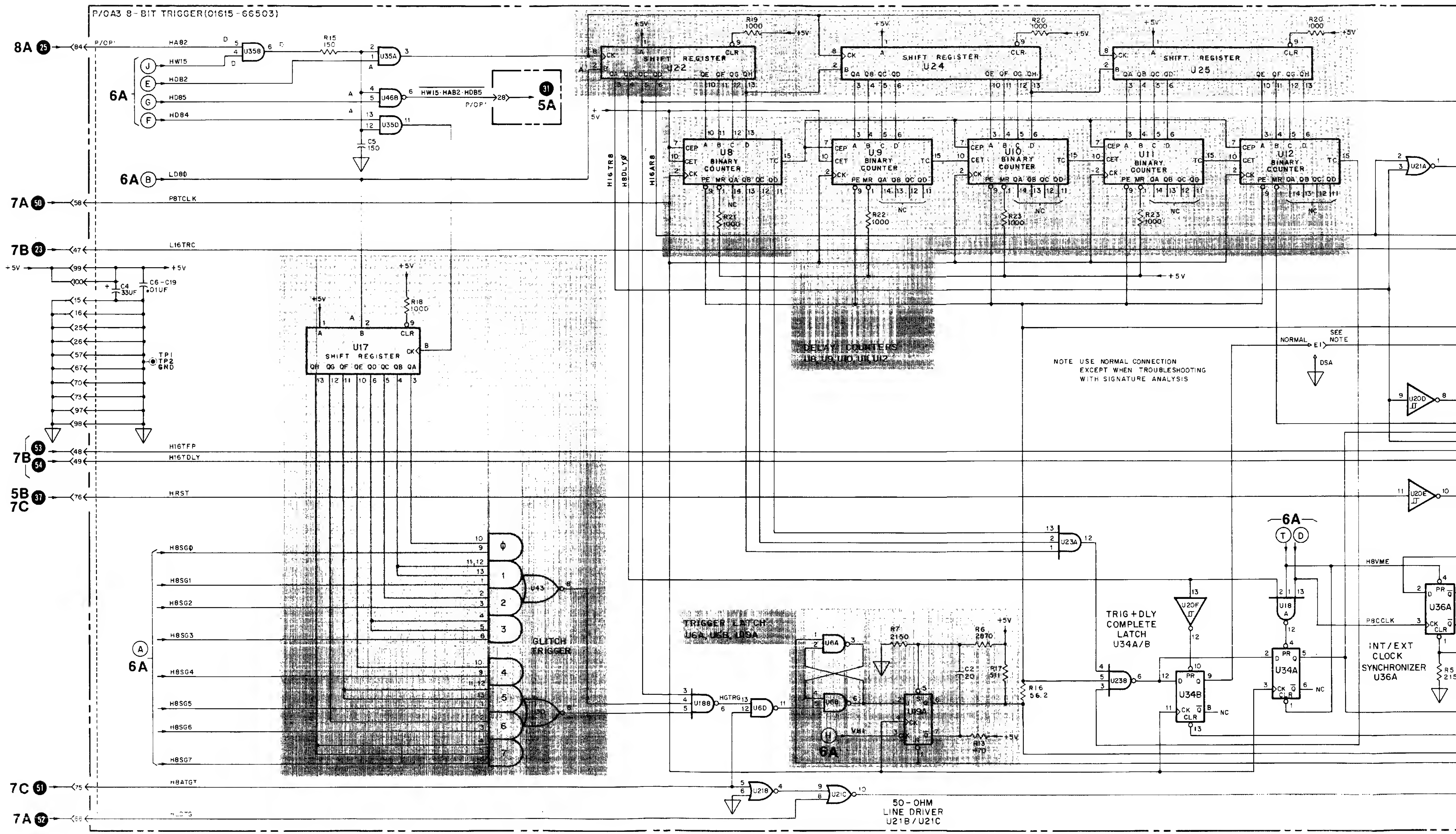
DSA jumper on A5 remains in NM (normal) position in this test setup.

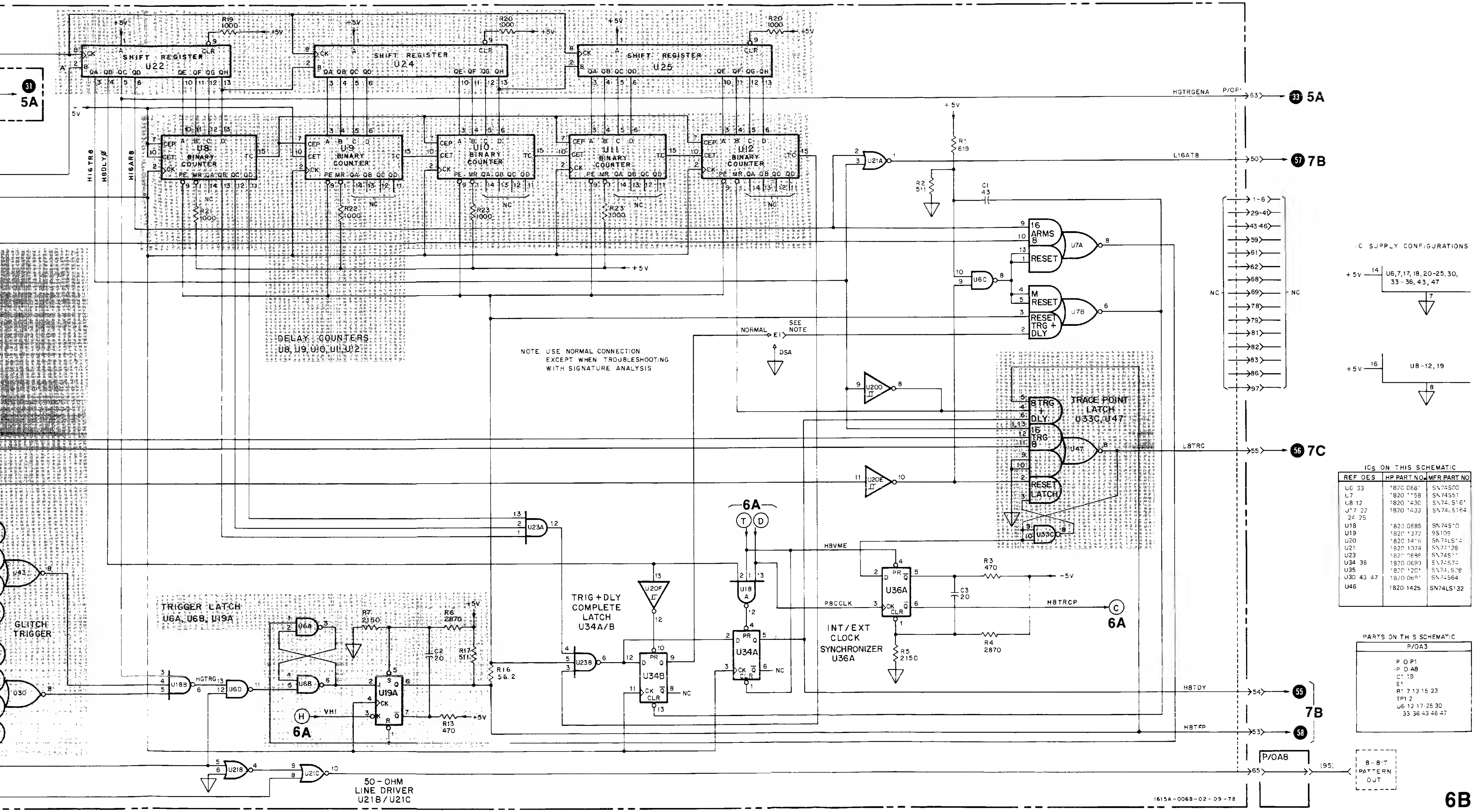
5. Set up signature analyzer as follows:

START .... ↑
STOP.................................... ↑
CLOCK.................................. ↑

Signatures for DSA Setup D (Schematic 6B)

Pin	Signature
VH A3U1-16	0001
A3U35-4	755P
A3U35-5	CCCA
A3U35-6	CPC5


P/OA3 8-BIT TRIGGER (01615-66503)
SHIFT REGISTER U22
SHIFT REGISTER U24
SHIFT REGISTER U25
U8 BINARY COUNTER
U9 BINARY COUNTER
U10 BINARY COUNTER
U11 BINARY COUNTER
U12 BINARY COUNTER
DELAY COUNTERS U8, U9, U10, U11, U12
U17 SHIFT REGISTER
GLITCH TRIGGER
TRIGGER LATCH U6A, U6B, U19A
TRIG + DLY COMPLETE LATCH U34A/B
INT/EXT CLOCK SYNCHRONIZER U36A
50-OHM LINE DRIVER U21B/U21C
NOTE USE NORMAL CONNECTION EXCEPT WHEN TROUBLESHOOTING WITH SIGNATURE ANALYSIS
NORMAL
SEE NOTE
DSA
HW15·HAB2·HDB5
P/OP'
PBTCLK
L16TRC
H16TFP
H16TDLY
HRST
H8SG0
H8SG1
H8SG2
H8SG3
H8SG4
H8SG5
H8SG6
H8SG7
H8ATGT
HGTRG
H8VME
P8CCLK
LD80
H16TR8
H8DLY0
H16AR8
8A
6A
5A
7A
7B
5B
7C



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U6, 33	1820-0681	SN74S00
U7	1820-1158	SN74S51
U8-12	1820-1430	SN74LS161
U17, 22, 24, 25	1820-1433	SN74LS164
U18	1820-0685	SN74S10
U19	1820-1372	9S109
U20	1820-1416	SN74LS14
U21	1820-1074	SN74128
U23	1820-0686	SN74S11
U34, 36	1820-0693	SN74S74
U35	1820-1201	SN74LS08
U30, 43, 47	1820-0691	SN74S64
U46	1820-1425	SN74LS132

Figure 8-37.
Timing Trigger (P/O A3) Schematic

SERVICE SHEET 7A

PRINCIPLES OF OPERATION

Internal Clock Generation. Y1 and associated circuitry comprise a 20-MHz oscillator which originates all internal clocks in the 1615A. U18 and U19A comprise a divide by 2, 5, and 10 network which obtains the frequencies for development of all internal clocks. Prior to each trace, the microprocessor supplies U3 with an 8-bit binary word on HDB0. These eight bits select a specific trigger mode and internal trigger frequency according to the operators menu selections. When pin 13 of U3 is high, U19A divides the 20-MHz oscillator output by 2, supplying the clock through U17D and U37D. This signal also parallel enables U18 after every pulse to reset the counter.

When pin 12 of U3 is high (and pin 13 low), U19A divides the 20-MHz signal by 5, parallel enabling U18 after every fifth clock.

Divide-by-10 is obtained by placing lows on pins 12 and 13 of U3. This disables U19A. The terminal count from U18 is the clock signal.

Asynchronous ripple counters U5, U6, and U7 are six divide-by-10 stages. Multiplexer U4 selects one of the clock frequencies from the ripple counters according to a three-bit code from U3. This is the asynchronous internal clock supplied through U28D and U41D.

External Clock. The PECLK and NECLK (Positive and Negative External Clocks) from the clock pod enter A2 as a differential signal. They are buffered and/or inverted through U41B and supplied to U40A and U40B. U2A controls U39A and U39B which select either the positive or negative edge of the external clock for strobe generation.

Microprocessor Clock. Prior to the start of a trace, the microprocessor generates a series of clocks to load the trigger memories in the 16-bit and 8-bit data-acquisition circuits. During this time, the microprocessor cuts off the internal and external clocks by setting HLDTG (High Load Triggers) high and H8ECLK (High 8-bit External Clocks) low from pins 3 and 4 of U3. The high HLDTG through U37C disables U4. HLDTG also forces pin 14 of U2C high to disable U40B. The low H8ECLK is inverted by U2B to disable U40A.

The microprocessor clocks are decoded by U51A through U51C. U43C and U43D supply the trigger-load clocks to the trigger memories in the 16-bit and 8-bit data-acquisition circuits. R58, R59, C27, and C28 protect against static discharge and provide proper signal levels for the TTL-to-ECL translators. U42A and U39C are enabled by inverting HLDTG through U2C. These gates supply the clocks that increment the counters in the data-acquisition circuitry to address the trigger memories. When the trigger memories have been fully loaded, HLDTG is set low. This stops the microprocessor clocks and enables the internal and external clock circuitry (U4, U40A, and U40B) for data acquisition.

Prerun Reset Period. After the microprocessor loads the trigger memories to the requirements of the menu, HRST (High Reset) switches high for 900 ns. During the HRST period, all glitch capture circuitry is initialized, and U2C places a 900-ns high on the D inputs of U15A and U15B to prevent generation of strobe pulses. When HRST switches low again, the D inputs of U15A and U15B are enabled and the 16-bit and 8-bit strobes begin.

Strobe Generation. The wire-ORed clock for the 8-bit machine (from U40A or U41D) clocks in the low D input of U15A. This resets the Q output, starting a negative-going charge on C7. The rate at which C7 charges toward -5.2 V is controlled by R10 and R6.

When the voltage on C7 is sufficiently negative, U1C provides a positive step output. This clocks U14B and sets U15A, returning the Q output high. This positive step is also gated through U39D and U42D to initialize the glitch-detection circuitry on assembly A4. R10 is adjusted to delay generation of the positive step from U1C by exactly 21 ns after receipt of the clock on U15A. This 21-ns delay is sufficient to allow all circuitry within the 1615A to be ready for the arrival of the 8-bit strobe.

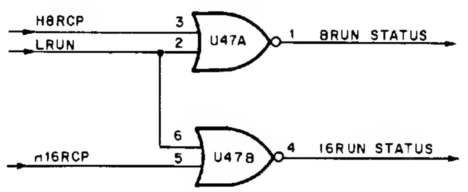
U14B and U1A, along with R11, R7, and C8 form the same type of circuit just described. R54 is added to aid recovery time. The 8-bit strobe is taken from the $\overline{Q}$ output of U14B. R11 is adjusted for a $\overline{Q}$ pulse period ending 49.5 ns after arrival of the 8-bit clock at U15A. This is the 8-bit clock strobe applied to clock gates U44 and U45, and delay gate U46.

When HRST is low (after the prerun reset period), the D input of U15B is low. U15B is clocked by P16SCLK(ECL). This resets U15B, driving the Q output low (inactive). Now pin 13 of U1D receives a negative-going charge from R12, R9, and C9. Pin 12 of U1D receives one-half of VBB(ECL). R12 is adjusted to obtain a 21-ns delay before this negative-going level crosses the threshold in U1D. Then U1D switches high, clocking U14A and setting U15B to initial conditions so that it will respond to the next P16SCLK(ECL).

U14A receives a low on the D input (except during the trigger load period before each run). U14A provides a high Q output each time it receives a positive edge from U1D. This high activates U27B which starts the 16-bit strobe. The feedback loop from U1B to U14A is delayed by R8, R13, and C10. R13 is adjusted for a 49.5-ns strobe period. Then U14A is set and its Q output returns low.

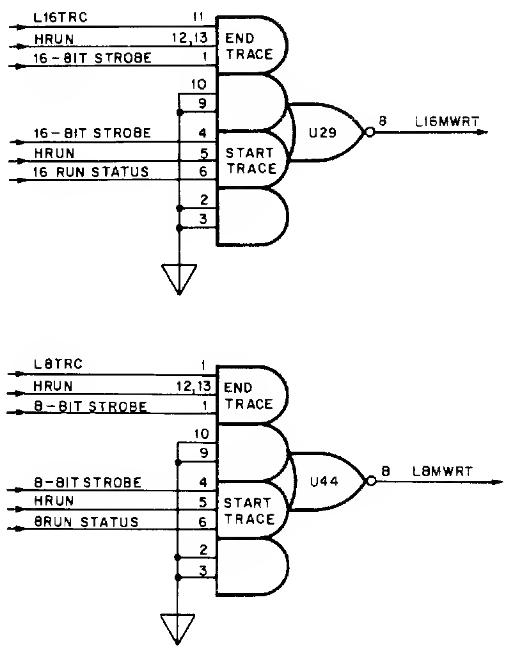
Test points TP2 and TP4 are used for measuring pulse delay and pulse period when making strobe adjustments.

Clock Gate Control. When HRST (High Reset) switches low, it clocks run/halt flip-flop U48A. With pin 5 of U48A switched high and pin 6 low, the output gates are enabled to supply clocks to the memories, memory address and index counters, and the trigger and delay circuits for 8-bit and 16-bit data acquisition. At the end of a trace for data acquisition, U37C clears U48A. This stops the data acquisition clocks and enables gates in U30 and U45 so that the microprocessor can supply clocks to read the memories when presenting a display.



Run Status Gates

Memory Write Clocks. See simplified diagram. U44 supplies memory-write clocks to the 8-bit memory. It operates only during a trace which includes 8-bit data acquisition. The end-trace AND function is enabled during end-display modes. It supplies clocks from the moment that the trace begins (HRUN switches high) and stops when the specified trigger plus delay is recognized (L8TRC switches low). The other AND function is enabled during start-display modes. It supplies clocks from the beginning of the run (HRUN switches high) and continues until the 8-bit memory is filled with valid data (8RUNSTAT switches low). U29 performs the same function for the 16-bit data acquisition.



Memory Write Clock Generator

Memory Address and
clocks to increment
(MAC) and memory
gates are used for ea
display, memory re
and memory read fo
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start-trace AND fun
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that were supplied t
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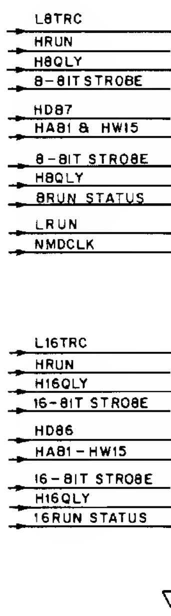
gates to hold off da
requirements are me
a data-acquisition r
is cleared, disabling
functions.



MIC and

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ries. When the trigger memories have been fully loaded, HLDTG is set low. This stops the microprocessor clocks and enables the internal and external clock circuitry (U4, U40A, and U40B) for data acquisition.

Prerun Reset Period. After the microprocessor loads the trigger memories to the requirements of the menu, HRST (High Reset) switches high for 900 ns. During the HRST period, all glitch capture circuitry is initialized, and U2C places a 900-ns high on the D inputs of U15A and U15B to prevent generation of strobe pulses. When HRST switches low again, the D inputs of U15A and U15B are enabled and the 16-bit and 8-bit strobes begin.

Strobe Generation. The wire-ORed clock for the 8-bit machine (from U40A or U41D) clocks in the low D input of U15A. This resets the Q output, starting a negative-going charge on C7. The rate at which C7 charges toward -5.2 V is controlled by R10 and R6.

When the voltage on C7 is sufficiently negative, U1C provides a positive step output. This clocks U14B and sets U15A, returning the Q output high. This positive step is also gated through U39D and U42D to initialize the glitch-detection circuitry on assembly A4. R10 is adjusted to delay generation of the positive step from U1C by exactly 21 ns after receipt of the clock on U15A. This 21-ns delay is sufficient to allow all circuitry within the 1615A to be ready for the arrival of the 8-bit strobe.

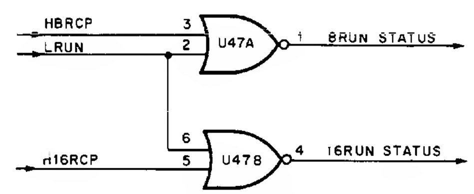
U14B and U1A, along with R11, R7, and C8 form the same type of circuit just described. R54 is added to aid recovery time. The 8-bit strobe is taken from the $\overline{Q}$ output of U14B. R11 is adjusted for a $\overline{Q}$ pulse period ending 49.5 ns after arrival of the 8-bit clock at U15A. This is the 8-bit clock strobe applied to clock gates U44 and U45, and delay gate U46.

When HRST is low (after the prerun reset period), the D input of U15B is low. U15B is clocked by P16SCLK(ECL). This resets U15B, driving the Q output low (inactive). Now pin 13 of U1D receives a negative-going charge from R12, R9, and C9. Pin 12 of U1D receives one-half of VBB(ECL). R12 is adjusted to obtain a 21-ns delay before this negative-going level crosses the threshold in U1D. Then U1D switches high, clocking U14A and setting U15B to initial conditions so that it will respond to the next P16SCLK(ECL).

U14A receives a low on the D input (except during the trigger load period before each run). U14A provides a high Q output each time it receives a positive edge from U1D. This high activates U27B which starts the 16-bit strobe. The feedback loop from U1B to U14A is delayed by R8, R13, and C10. R13 is adjusted for a 49.5-ns strobe period. Then U14A is set and its Q output returns low.

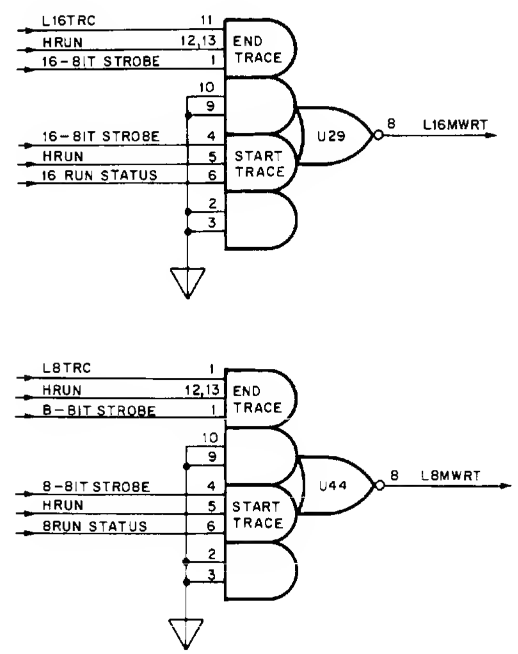
Test points TP2 and TP4 are used for measuring pulse delay and pulse period when making strobe adjustments.

Clock Gate Control. When HRST (High Reset) switches low, it clocks run/halt flip-flop U48A. With pin 5 of U48A switched high and pin 6 low, the output gates are enabled to supply clocks to the memories, memory address and index counters, and the trigger and delay circuits for 8-bit and 16-bit data acquisition. At the end of a trace for data acquisition, U37C clears U48A. This stops the data acquisition clocks and enables gates in U30 and U45 so that the microprocessor can supply clocks to read the memories when presenting a display.



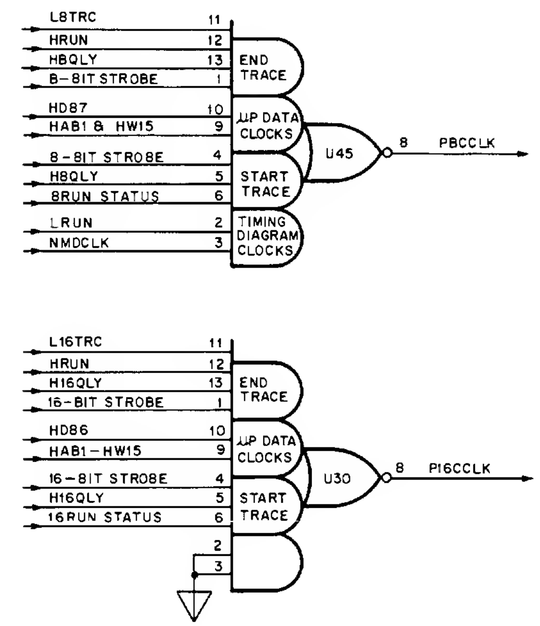
Run Status Gates

Memory Write Clocks. See simplified diagram. U44 supplies memory-write clocks to the 8-bit memory. It operates only during a trace which includes 8-bit data acquisition. The end-trace AND function is enabled during end-display modes. It supplies clocks from the moment that the trace begins (HRUN switches high) and stops when the specified trigger plus delay is recognized (L8TRC switches low). The other AND function is enabled during start-display modes. It supplies clocks from the beginning of the run (HRUN switches high) and continues until the 8-bit memory is filled with valid data (8RUNSTAT switches low). U29 performs the same function for the 16-bit data acquisition.



Memory Write Clock Generator

Memory Address and Index Counter Clocks. U45 supplies clocks to increment the 8-bit memory address counter (MAC) and memory index counter (MIC). Separate AND gates are used for each of four modes: start display, end display, memory read for alphanumeric presentation, and memory read for timing diagram presentation. During a trace for data acquisition, either the end-trace or start-trace AND function will generate the clocks. These two functions receive basically the same input signals that were supplied to their counterparts in the memory-write clock generator. H8QLY is added to these AND gates to hold off data acquisition until clock qualifier requirements are met, if selected in the 8-bit menu. After a data-acquisition run is complete, the run/halt flip-flop is cleared, disabling the start-trace and end-trace AND functions.



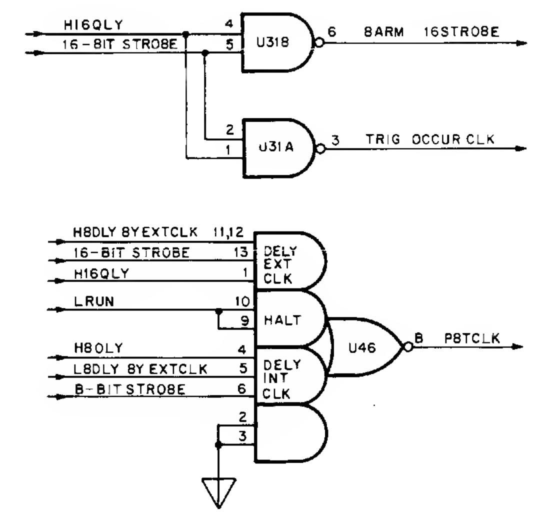
MIC and MAC Clock Generator

To read the 8-bit memory for presenting a timing diagram, the microprocessor supplies a number of NMDCLK clocks to one AND function in U45. These clocks increment the 8-bit memory address counter. Since no memory-write clocks occur at this time, data in the 8-bit memory is unaffected. The microprocessor uses a different AND function in U45 to supply clocks when presenting alphanumeric displays. HAB1 is ANDed with HW15 to enable this AND function, and the clocks are supplied via data bus line HDB7.

U30 provides the same functions for the 16-bit memory address and index counters. The gate used for timing diagram clocks in U45 is disabled in U30.

Trigger Plus Delay Clock Generators. U46 supplies clocks to the 8-bit trigger and delay circuitry. These clocks are used to latch in trigger recognition and to increment the 8-bit delay counters when trigger plus delay is selected. One AND function in U46 is enabled when counting internal clocks to obtain a time delay. Another AND function in U46 is used when counting delay by a number of external clocks. A third AND function is used to ensure that U46 is disabled except during data-acquisition runs.

The clocks used in the 16-bit circuitry to latch in trigger recognition and to increment the 16-bit delay counters are supplied by U31A and U31B.



Trigger Plus Delay Clocks

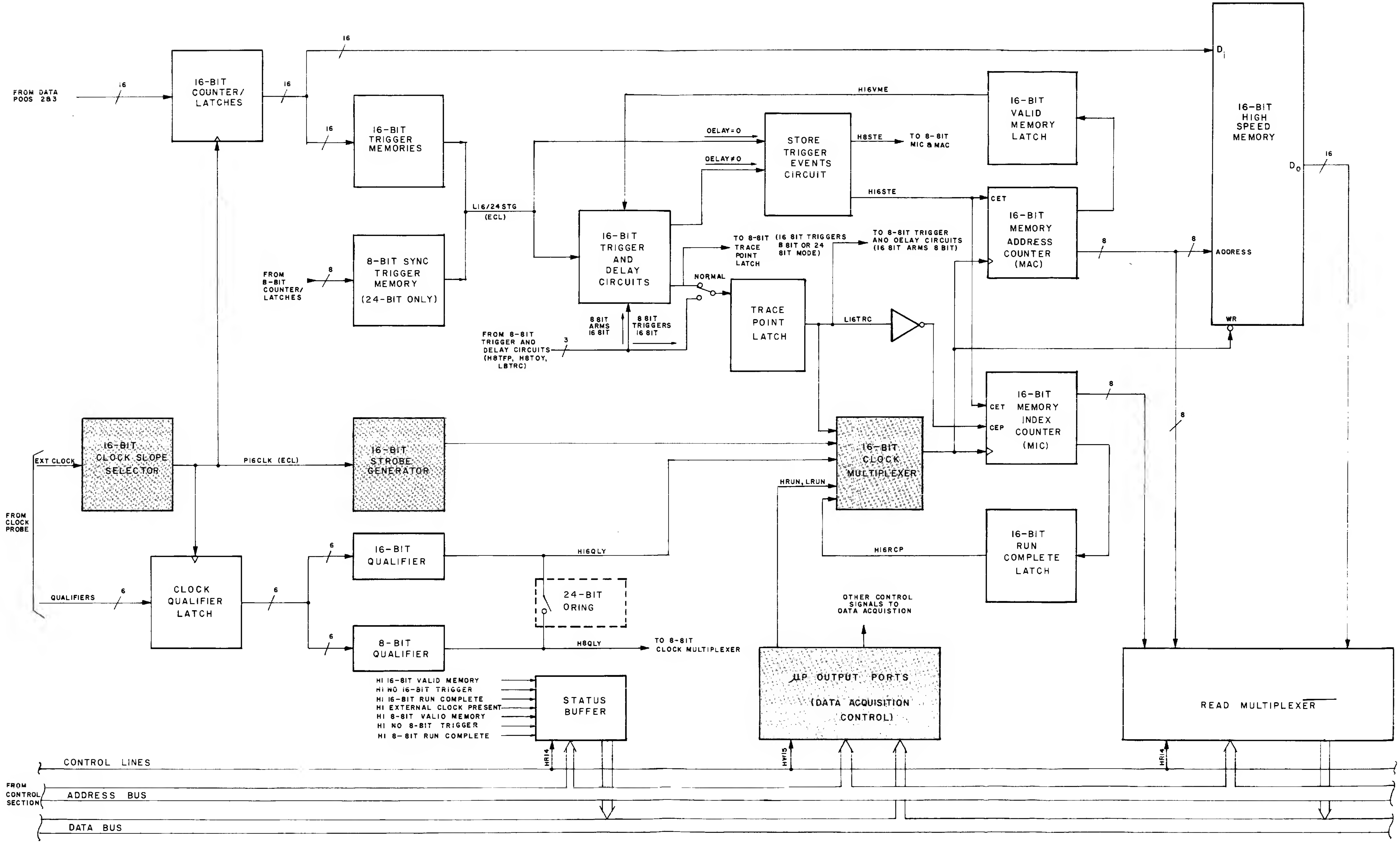


Figure 8-38.
Block Diagram, 16-bit Data-acquisition Section for Schematic 7A

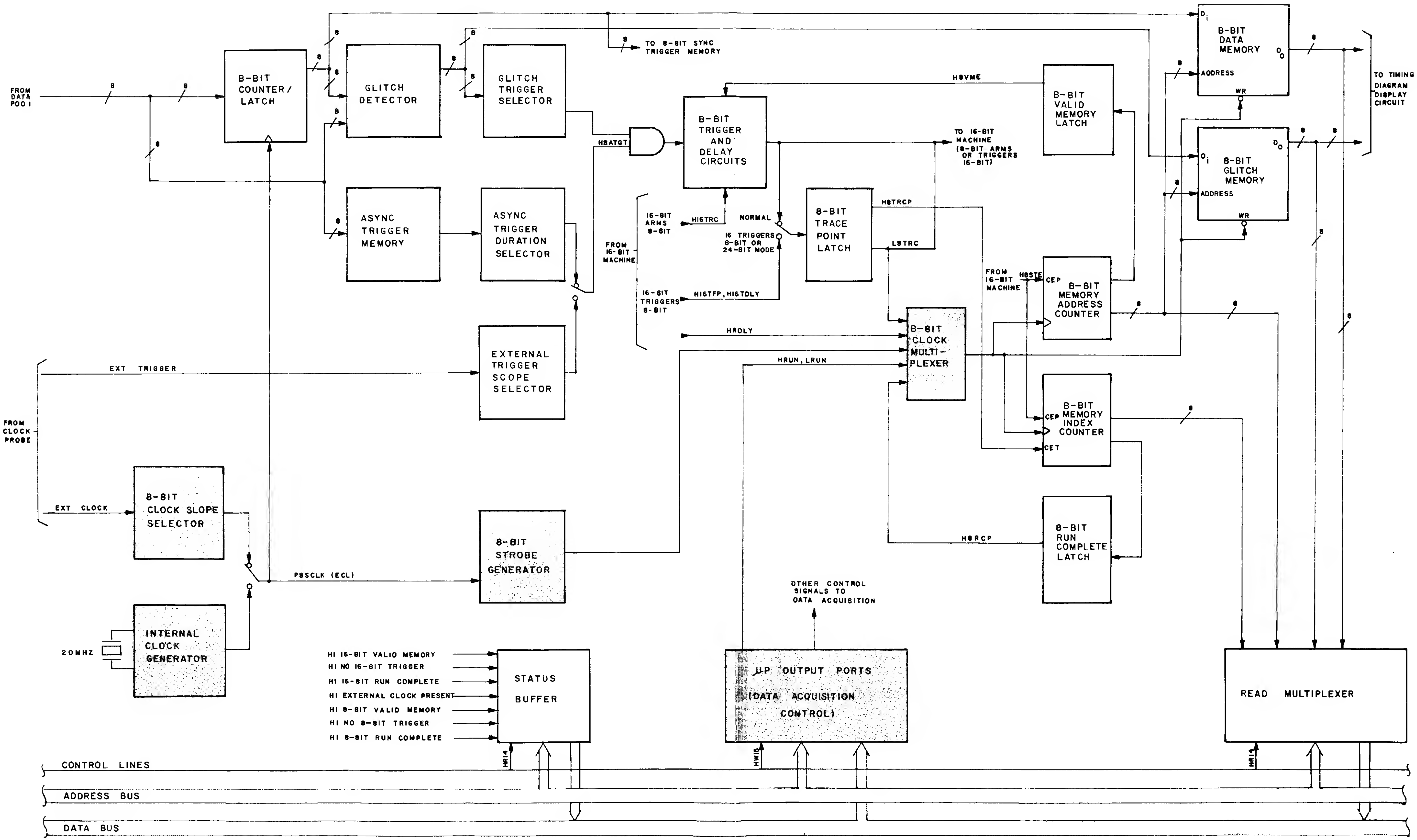


Figure 8-39. Block Diagram, 8-bit Data-acquisition Section for Schematic 7A

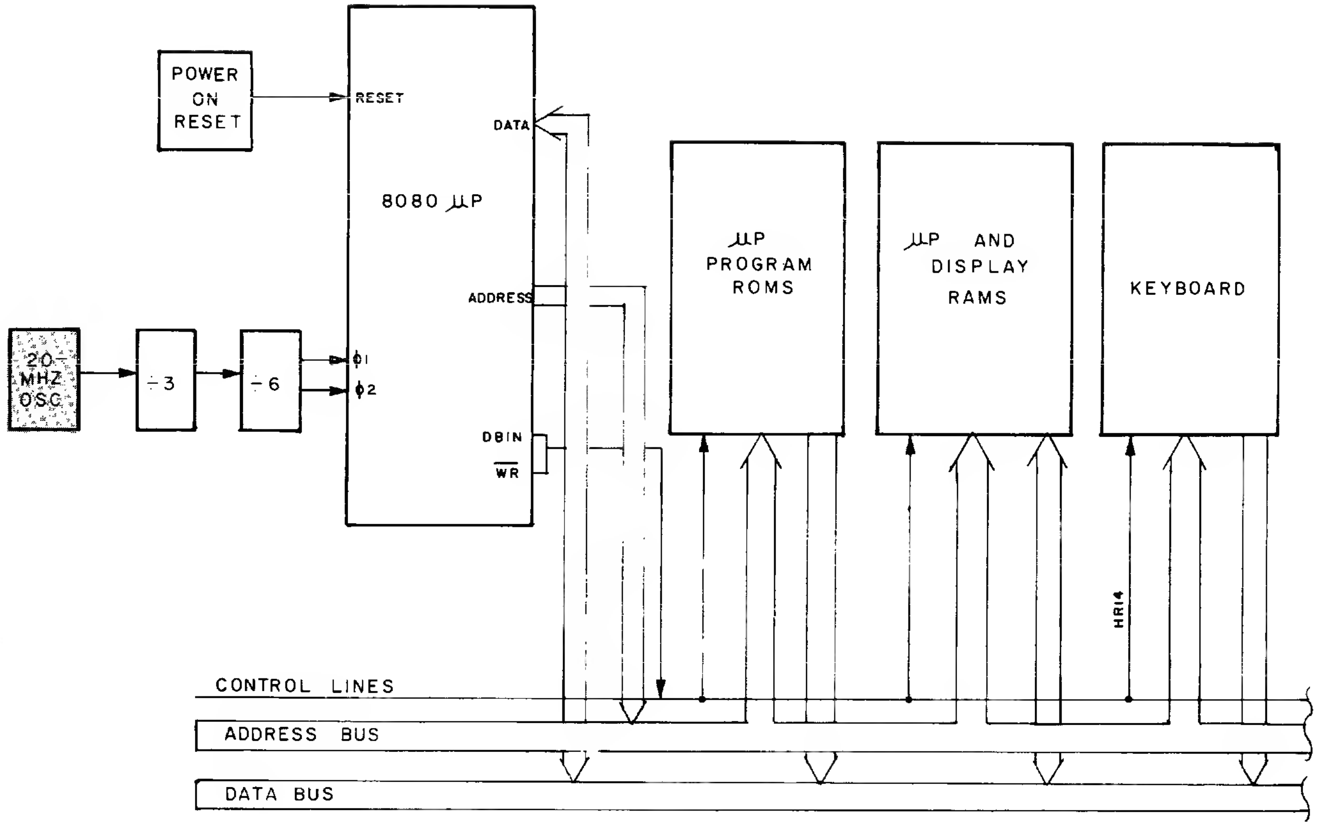


Figure 8-40. Block Diagram, Control Section for Schematic 7A

IC'S on Schematic 7A

Ref Des	HP Part No.	Mfr Part No.
U1	1820-0809	MC10115P
U2	1820-1173	MC10124L
U3	1820-1433	SN74LS164N
U4	1820-1217	SN74LS151N
U5,6,7	1820-1991	SN74LS390N
U14,15	1820-1225	MC10231P
U17	1820-0683	SN74S04N
U18	1820-1992	AM25LS160PC
U19	1820-1158	SN74S51N
P/O U25	1820-1730	SN74LS273N
U27	1820-2010	1820-2010
U28,43	1820-1173	MC10124L
U29,30,44-46	1820-0691	SN74S64N
U31	1820-0681	SN74S00N
U37	1820-1449	SN74S32N
U39	1820-1831	MC10103L
U40	1820-1946	MC10117L
U41	1820-1320	MC10216L
U42	1820-0802	MC10102P
U47	1820-1322	SN74S02N
U48	1820-0629	SN74S112N
U51	1820-1201	SN74LS08N
U52	1820-1425	SN74LS132N

Parts on Schematic 7A

A2	A1	A4	A8	Chassis
C4-13,27,28,30	R57	R21	XA1 XA2	P/O J8 P/O W4
R1-23,25,30,31, 42,46-48,54, 55,58,59,61,65 69,70 TP2,4,7 U1-7,14,15,17-19, P/O U25,27-31,37, 39-48,51,52 54-57 Y1	P/O P3, P/O P4			

SIGNATURE ANALYSIS FOR SCHEMATIC 7A.

The signatures on this schematic are obtained by using DSA Setups A and D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A2 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A2, and install A2 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ↓
STOP .... ↑
CLOCK .... ↓

Signatures for DSA Setup A (Schematic 7A)

Pin	Signature
VH A2U3-14	C690
A2U3-2	FHPA
A2U30-10	FA2P
A2U45-10	427H
A2U51-5	FA2P
A2U51-10	427H

DSA SETUP D.

1. Remove assembly A2 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A2 and install A2 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   c. Connect signature analyzer stop line to same point as start line, step b above.

   d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{WR}$ line.

4. Reinstall A5 in 1615A mainframe.

NOTE

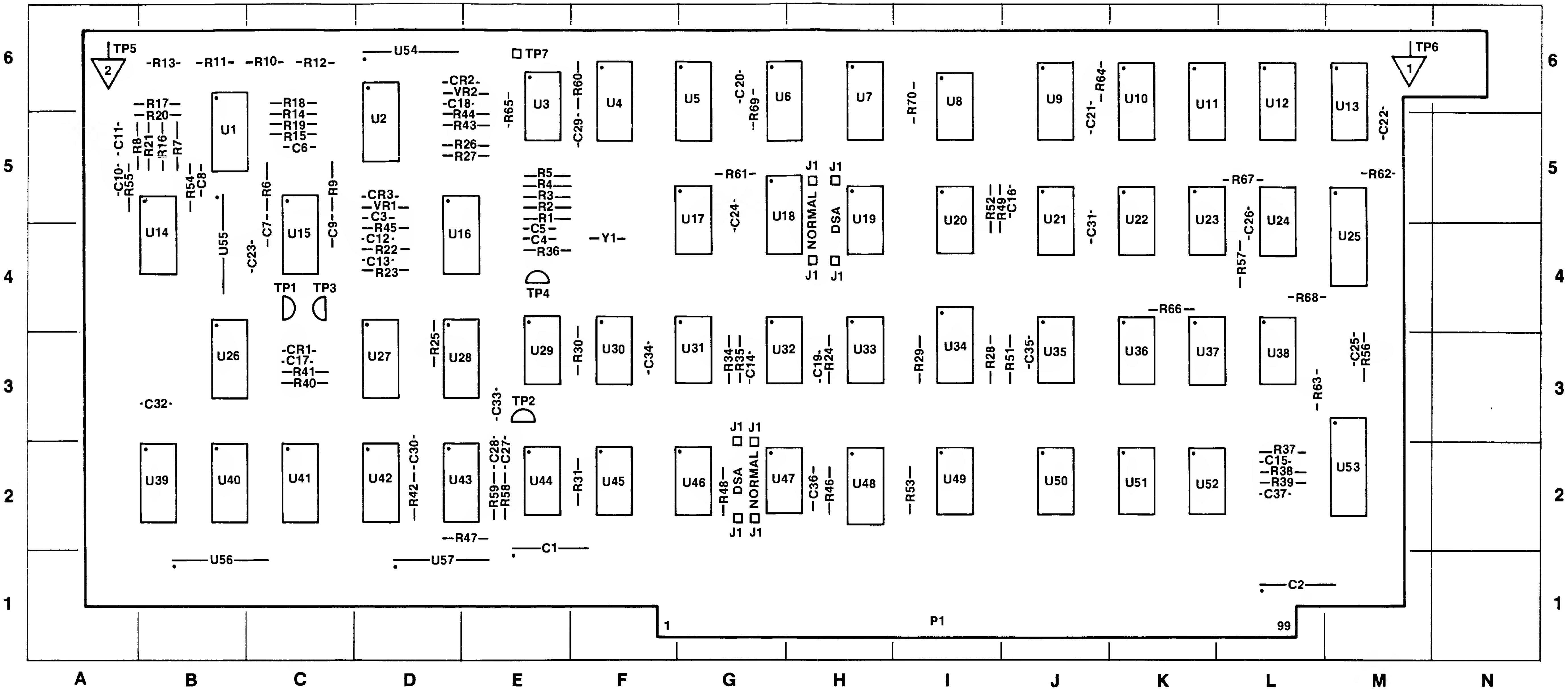
DSA jumper on A5 remains in NM (normal) position in this test setup.

5. Set up signature analyzer as follows:

START .... ↑
STOP .... ↑
CLOCK .... ↑

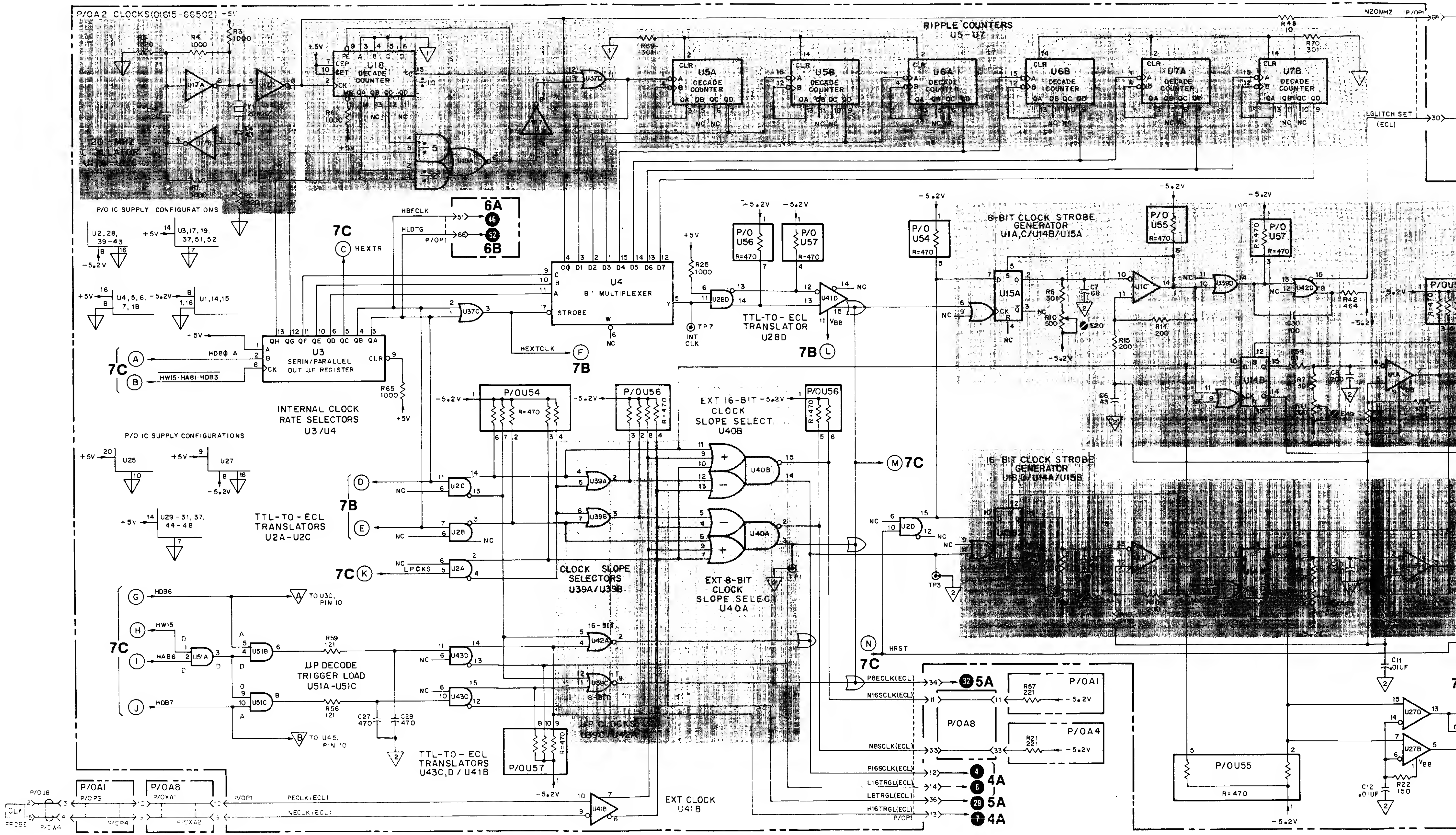
Signatures for DSA Setup D (Schematic 7A)

Pin	Signature
VH A2U3-14	0001
A2U30-9	9118
A2U51-1	755P
A2U51-2	UPFF
A2U51-3	U982
A2U51-4	U982
A2U51-9	U982



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C19	H-3	C37	L-2	R14	C-5	R34	G-3	R53	I-2	R70	I-6	U10	K-6	U27	D-3	U44	E-2
C2	L-1	C20	C-6	CR1	C-3	R15	C-5	R35	G-3	R54	B-4	TP1	C-4	U11	K-6	U28	D-3	U45	F-2
C3	D-5	C21	J-5	CR2	D-6	R16	B-5	R36	E-4	R55	A-5	TP2	E-3	U12	L-6	U29	E-3	U46	G-2
C4	E-4	C22	M-5	CR3	D-5	R17	B-6	R37	L-2	R56	M-3	TP3	3-4	U13	M-6	U30	F-3	U47	G-2
C5	E-4	C23	C-4	P1	I-1	R18	C-6	R38	L-2	R57	L-4	TP4	E-4	U14	B-4	U31	G-3	U48	H-2
C6	C-5	C24	G-5	R1	E-5	R19	C-5	R39	L-2	R58	E-2	TP5	A-6	U15	C-4	U32	G-3	U49	I-2
C7	C-4	C25	M-3	R2	E-5	R20	B-5	R40	C-3	R59	E-2	TP6	M-6	U16	D-4	U33	H-3	U50	J-2
C8	B-5	C26	L-5	R3	E-5	R21	B-5	R41	C-3	R60	F-6	TP7	E-6	U17	G-5	U34	I-3	U51	K-2
C9	C-4	C27	E-2	R4	E-5	R22	D-4	R42	D-2	R61	G-5	U1	B-5	U18	G-5	U35	J-3	U52	K-2
C10	A-5	C28	E-2	R5	E-5	R23	D-4	R43	E-5	R62	M-5	U2	D-5	U19	H-5	U36	K-3	U53	M-2
C11	A-5	C29	F-5	R6	C-5	R24	H-3	R44	E-5	R63	L-3	U3	E-6	U20	I-5	U37	K-3	U54	D-6
C12	D-4	C30	D-2	R7	8-5	R25	D-3	R45	D-4	R64	J-6	U4	F-6	U21	J-5	U38	L-3	U55	B-4
C13	D-4	C31	J-4	R8	A-5	R26	E-5	R46	H-2	R65	E-6	U5	G-6	U22	K-5	U39	8-2	U56	B-1
C14	G-3	C32	B-3	R9	C-5	R27	E-5	R47	E-2	R66	K-4	U6	G-6	U23	K-5	U40	8-2	U57	D-1
C15	L-2	C33	E-3	R10	C-6	R28	I-3	R48	G-2	R67	L-5	U7	H-6	U24	L-5	U41	C-2	VR1	D-5
C16	J-5	C34	F-3	R11	B-6	R29	I-3	R49	I-5	R68	L-4	UB	I-6	U25	M-4	U42	D-2	VR2	E-6
C17	C-3	C35	J-3	R12	C-6	R30	F-3	R51	J-3	R69	G-6	U9	J-6	U26	B-3	U43	D-2	Y1	F-4
C18	D-6	C36	H-2	R13	B-6	R31	F-2	R52	I-5										

Figure 8-41. Trigger and Clock Assembly A2, Parts Identification


P/OA2 CLOCKS(01615-66502)
RIPPLE COUNTERS
U5-U7
20-MHZ OSCILLATOR U17A-U2C
P/O IC SUPPLY CONFIGURATIONS
INTERNAL CLOCK
RATE SELECTORS
U3/U4
U3
SERIN/PARALLEL
OUT UP REGISTER
U4
8:1 MULTIPLEXER
TTL-TO-ECL
TRANSLATOR
U28D
8-BIT CLOCK STROBE
GENERATOR
U1A,C/U14B/U15A
16-BIT CLOCK STROBE
GENERATOR
U1B,D/U14A/U15B
EXT 16-BIT
CLOCK
SLOPE SELECT
U40B
EXT 8-BIT
CLOCK
SLOPE SELECT
U40A
CLOCK SLOPE
SELECTORS
U39A/U39B
TTL-TO-ECL
TRANSLATORS
U2A-U2C
UP DECODE
TRIGGER LOAD
U51A-U51C
TTL-TO-ECL
TRANSLATORS
U43C,D / U41B
UP CLOCKS
U39C/U42A
EXT CLOCK
U41B
HEXTR
HEXTCLK
HBECLK
HLDTG
LGLITCH SET (ECL)
N20MHZ
HRST
P8ECLK(ECL)
N16SCLK(ECL)
N8SCLK(ECL)
P16SCLK(ECL)
L16TRGL(ECL)
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7B
7C
5A
4A

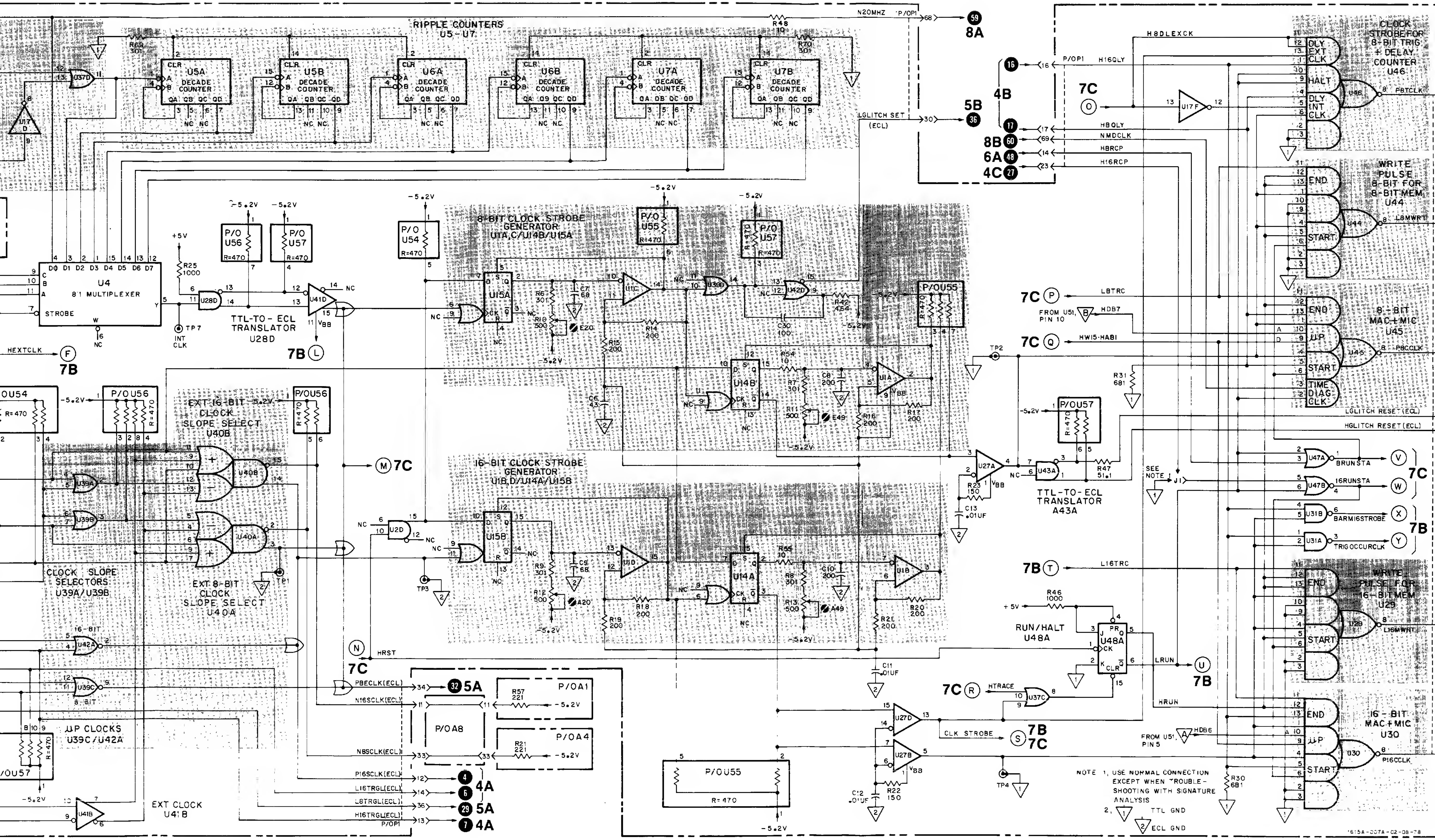


Figure 8-42.
Clocks (P/O A2) Schematic

SERVICE SHEET 7B

PRINCIPLES OF OPERATION

This portion of the circuitry generates the trigger that establishes trace point for a run of data acquisition in the state mode. When 16 bits of state information are to be captured, only the trigger memory on assembly A1 is monitored. When the 24-bit state mode is selected, the 16-bit trigger memory is ANDed with the 8-bit trigger memory on assembly A4. This ensures that all 24 bits in the trigger word will be true before generating L16/24STG(ECL) (Low 16/24-bit State Trigger, ECL).

When a specified state trigger is recognized, the trigger memories supply L16/24STG(ECL), activating U16A through U16D. When U16B activates, it places high states on the D input of U20A and the J input of U34A.

Trigger Occurrence Memory. The function of U34A is to remember that a trigger has been recognized at least one time during a trace. The high state from U16B is clocked into U34A, setting the Q output high. It remains high for the rest of the trace, performing many enable functions.

Trigger Delay Equal to 0. If the operator has chosen delay equal to 0, the microprocessor loads a high state on pin 4 of U22. This forces pin 8 of U21 low. When the selected trigger memories are valid, U50C switches low. This forces U47C high, releasing the clear input of U34B. The J input of U34B is always high, except when delaying by trigger occurrences. Therefore, the next qualified clock will issue H16TDLY (High 16-bit Time Delay) from U34B.

Pin 6 of U36 is always high, except in the 8-bit triggers 16-bit mode. When trigger recognition is clocked into U34A, the high Q output is applied to pin 5 of U36, completing the AND function, and generating L16TRC (Low 16-bit Trace Point).

Delay Register. Before beginning a data-acquisition run, the microprocessor loads the delay register with the trigger and delay selections made in the 16-bit or 24-bit state menu. U23, U24, and pins 10 through 13 of U22 contain a 24-bit number which represents terminal count minus delay in the delay counter. This is loaded into the delay counter during LRST, a 900-ns reset period from the microprocessor. LRST switches U31C output high, switching U19B low, clearing U20A and U34A.

The low state from U34A is applied to the parallel-enable inputs of U9 through U13, forcing them to load the delay state from the delay register during the rising edge of the first clock. After the trace begins and trigger recognition occurs, U34A switches its output high, releasing the parallel-enable inputs of the delay counter.

Delay Control. A high Q output from U20A enables the delay counter to count the delay period. The Q output of U20A is always high due to a low on pin 4, except when delay by trigger occurrences is selected. In this mode, U20A only enables the delay counter during clock periods which include a recognized trigger.

Delay Gate U21 and Associated Circuitry. The delay gate activates trigger, reset, and enable circuitry when it provides a low output. This low output is generated in one of three different ways, depending on the mode of trigger delay: during the entire run when delay = 0 is selected; after recognition of a related number of internal clocks when delay by time is selected; and after recognition of a number of trigger occurrences when delay by occurrences is selected. The logic for each of the three delay conditions is explained in the following paragraphs.

When delay equal to 0 is selected, pin 4 of U22 is high. This enables one AND function of U21, forcing its output low for the entire run.

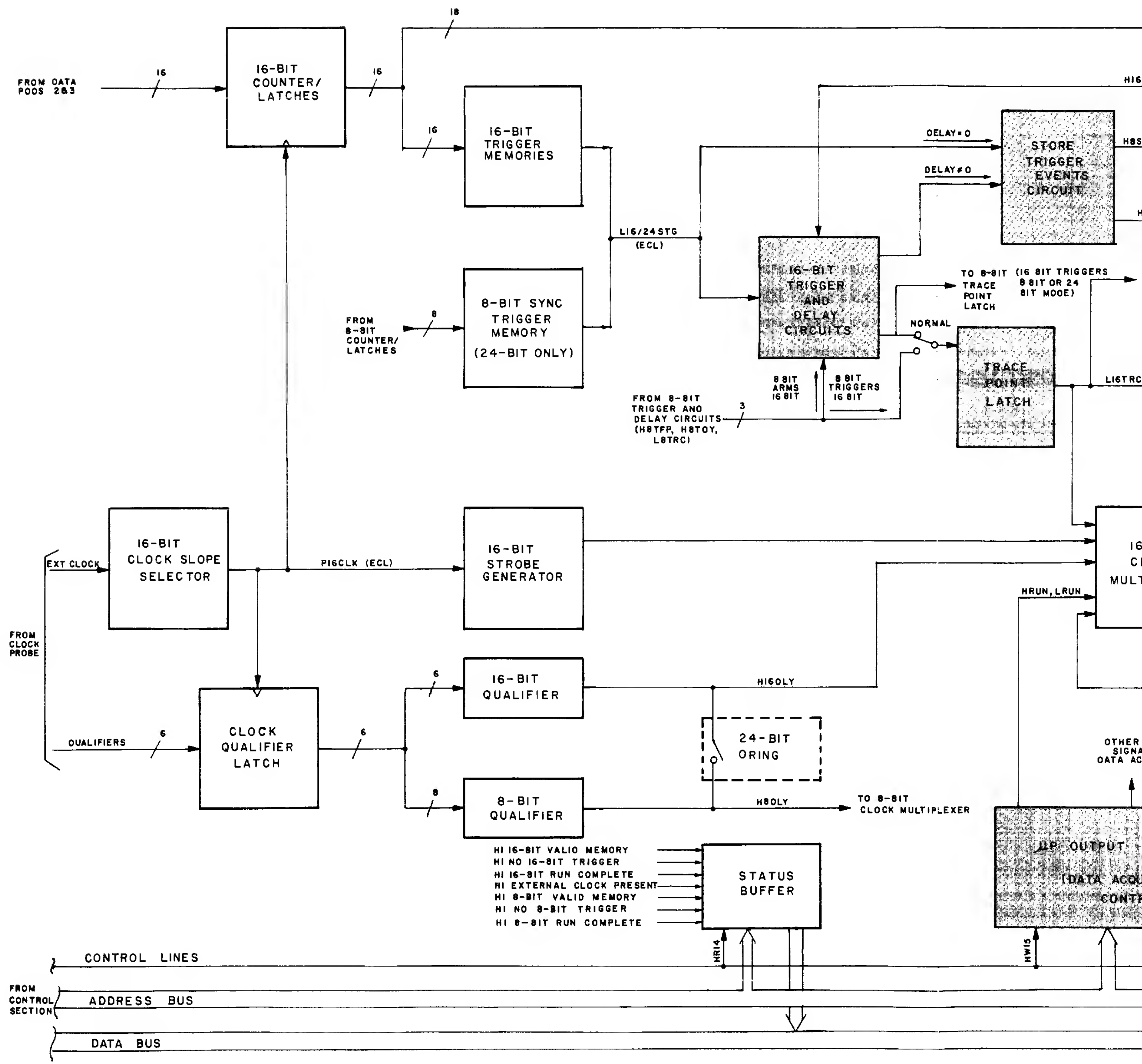
When delay not equal to 0 is selected, several outputs from the delay counter are applied to U21. U13 contains the four most significant bits in the delay counter. When these four bits are 1111 (terminal count), U13 supplies enable voltages to the two AND functions dedicated to time and occurrence delays.

U8B also supplies enable voltages to the same two AND functions. U8B delivers a high output on counts 14 and 15 in U9 (the least significant bit counter).

If trigger-occurrence delay is selected, then the top AND function in U21 is used. In this mode, the final enable is supplied by U8A. It decodes all odd numbered states from U9 and forces U21 low when U9 reaches count 15 and the output of U20A is high (next trigger recognition).

Delay Gate and Trace Point Circuitry. In delay by trigger occurrences, the output of U21 switches low at the end of the delay period established in the menu. In delay by clocks, the output of U21 switches low one clock before the end of the delay period established in the menu. In delay equal to 0, U21 output is low from the start of the trace due to a high state on pin 4 of U22.

The low output from U21 performs the following three functions: (1) it releases U47D (this removes the clear from U20B, enabling the reset function); (2) it releases U47C (this allows generation of a trigger through U34B as long as 8-bit and 16-bit valid memory conditions are correct); and (3) it forces U49A and U49B high (this provides H16STE and H8STE to enable the 8-bit and 16-bit memory counters for data acquisition.



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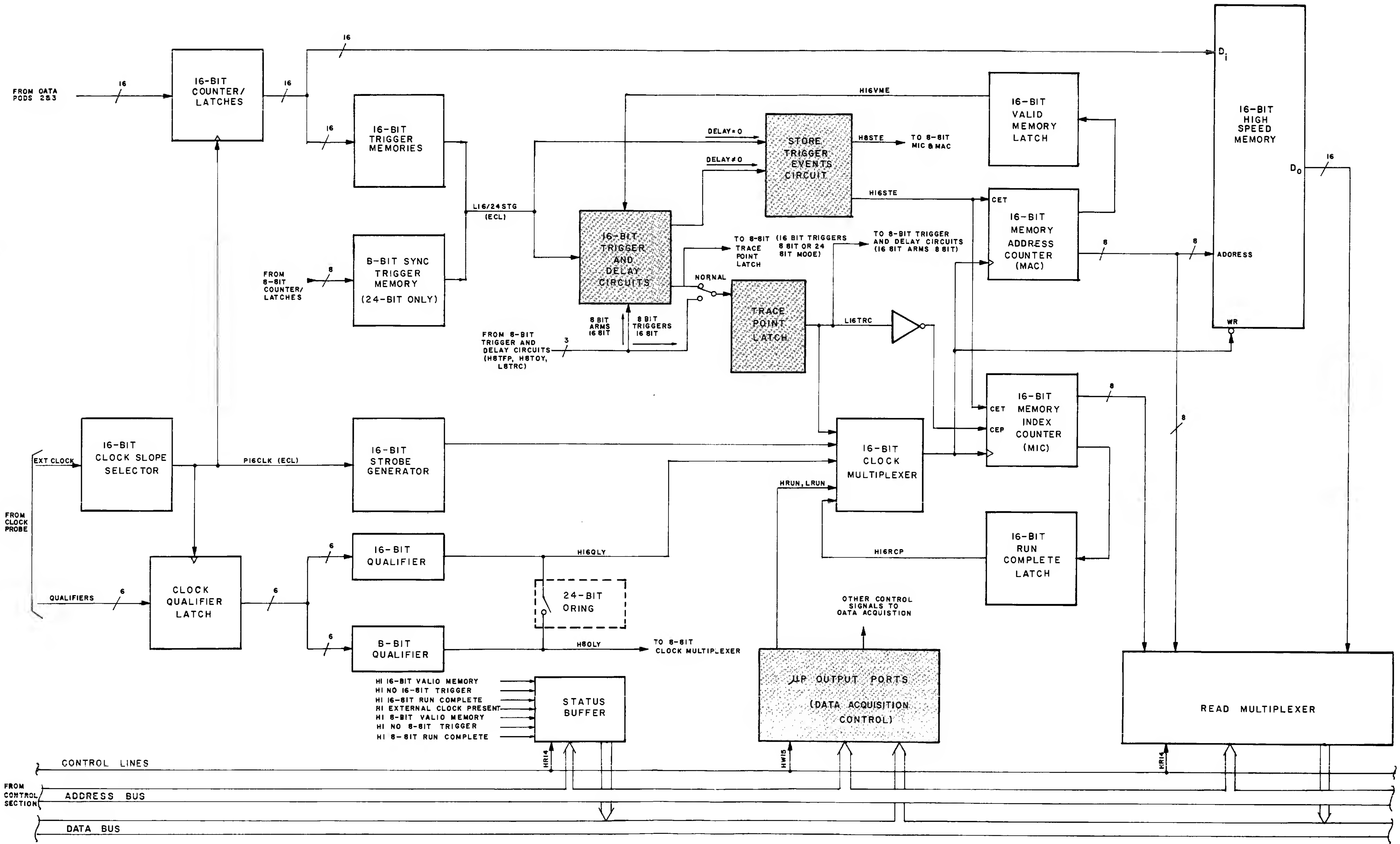


Figure 8-43. Block Diagram, 16-bit Data-acquisition Section for Schematic 7B

U34B sets when the trigger plus delay specification is met. This high output is supplied to A3 where it triggers the 8-bit machine in the 16-bit triggers 8-bit mode. It also enables one AND function in U36. When U20B sets, its Q output initiates the reset cycle through U33B.

Trigger Gate. U36 generates L16TRC (Low 16-bit Trace Point). This enables the 16-bit memory index counter to limit the contents of the state memory during START display modes. In END display modes, L16TRC stops the run. It also activates the 16-bit ARMS 8-bit AOI on A3. U36 generates L16TRC in the following three conditions:

1. When 16-bit trigger plus 16-bit delay specification is met in the state circuitry.

2. During 8 ARMS 16, after arming of the 8-bit is complete and the 16-bit trigger arrives.

3. When in 8 TRIG 16 mode and all 8-bit trigger requirements are met.

The low L16TRC is inverted through U31D and applied to pin 9 of U36. Pin 10 of U36 is high, except during microprocessor reset, so U36 maintains L16TRC until after the trace is complete. Pin 9 of U32C is set low at the beginning of a trace by the run/halt flip-flop. When U36 generates L16TRC, the high transition from U31D switches U32C low, providing the transition to the 16/24-bit TRACE OUT connector on the rear panel.

Reset Period and Oscilloscope Trigger Generation. U20B initiates the reset period. Its Q output switches high at the same instant that U34B generates H16TDLY. The high from U20B is applied to pin 10 of U33B. Pin 9 of U33B is high after trigger recognition in U34A so U33B switches low. Part of this low state initiates the oscilloscope trigger in U32A. Pin 3 of U32A is always low except when the microprocessor is loading the trigger memories. The low transition from U33B forces U32A to generate a positive-going trigger to the 16/24 BIT TRIG OUT connector on the rear panel. This is used for synchronizing an oscilloscope to observe electrical occurrences coincident with the 1615A trace point. U32A generates a new trigger every time the 1615A recognizes its trigger plus delay, even though U36 only initiates data acquisition the first time that the trace point is recognized.

The low reset transition from U33B is also coupled through C14 to switch U31C high. The high output from U31C forces U19B to clear U20A and U34A, parallel-enabling the delay counter to terminal count minus delay. U31C also clears U20B through U47D, preparing the circuitry to generate the next oscilloscope trigger when the next trace point occurs.

Valid Memory Recognition. Trigger plus delay flip-flop U34B is normally held in the cleared state either by a high from U21 (before the end of the selected delay), or by a high from U50C (when it detects that either the 16-bit or 8-bit data memories are not valid).

In all trigger modes except 16-bit arms/trigger 8-bit, U49C holds U48B in the preset state. This allows H16VME to control the holdoff of U34B through U50C and U47C. In START display modes, H16VME is high from the beginning of the run so U34B is released to the control of delay gate U21.

In END display modes, U34B is held in the cleared state by U50C until after a full 256 bytes of valid data has been captured in the 16-bit memory. To do this, H16 VME remains low until the 16-bit memory has advanced a full 256 counts. Then H16VME switches high, releasing U34B to the control of U21.

During 16-bit arms or triggers 8-bit modes, L16AT8 forces U49C high. This removes the preset state from U48B, preventing recognition of H16VME in U50C. H8VME will switch high only when the 8-bit memory is valid. This will be clocked into U48B. Then U50C will be able to recognize H16VME. This ensures that the 8-bit asynchronous memory and the 16-bit synchronous memory will both be valid before recognition of trace point. The 1615A can not display partial timing diagrams; without this additional holdoff, the 1615A would show a full timing diagram with no distinction between that portion of the diagram which contains valid data and that portion which would not contain valid data.

8 Arms 16 Logic. This circuit holds off 16-bit trigger recognition until after the 8-bit trace point has occurred. Prior to a run in this mode of triggering, the microprocessor sets pin 6 of U22 high. The LRST (Low Reset) period at the beginning of each run presets the Q output of U38A high. U19B ANDs these two high states and clears U20A and U34A, preventing trigger recognition and delay counting.

U33A is activated by the high state from pin 6 of U22 and the positive edge of the strobe generator pulse. It provides clock pulses to U38A. When the trace point is recognized in the 8-bit instrument, L8TRC switches low. This low is clocked into U38A, forcing the output of U19B high. This releases U20A and U34A to recognize the 16-bit trigger and start the delay counter. The $\overline{Q}$ of U38A enables the AND portion of U36 which responds to 8-bit triggers 16-bit mode with internal clock.

8 Triggers 16 Logic. This circuit allows the 8-bit trace point signal (L8TRC) to initiate the 16-bit trace point from U36 (L16TRC). Prior to a run in this mode of triggering, the microprocessor sets pin 3 of U22 high. U19B holds off trigger recognition and delay counting just as in 8 ARMS 16 mode.

U33A is activated by the high state from pin 3 of U22 and the negative edge of the strobe generator pulse. It supplies clocks to U38A. When L8TRC switches low (8-bit trace point occurs), U38A changes states. U36 ANDs

the high Q from U38A with the high state from pin 3 of U22 and generates L16TRC.

The bottom AND gate in U36 is enabled when the 8-bit triggers 16-bit mode is selected during use of an external clock. It ANDs the high 8 triggers 16 from pin 3 of U22 with the 8-bit trigger recognition and time delay from assembly A3.

Delay by Trigger Occurrences. In this mode, the microprocessor sets pin 5 of U22 high prior to run start. This removes the preset from U20A. The Q output of U20A is only clocked high after each trigger recognition, and clocked low again during periods of nontrigger recognition. This allows the delay generator to count only those clocks that occur immediately after each trigger recognition.

Pin 11 of U17E also receives the high from pin 5 of U22. This forces pin 10 low, cutting off VR1. Now U16D places a high state on the inputs of U34B and U20B only during those clock periods which include a recognized trigger. This prevents generation of L16TRC during other clock periods.

24-bit Trace Events with Delay = 0 Logic. The microprocessor sets pin 4 of U22 high before starting a run in this mode. This enables U16A and U16C by connecting them to V_{BB} through U35C. In this condition, U16A and U16C provide high outputs only when a trigger is recognized. Their high states are connected through hot-carrier diodes to the count-enable-parallel inputs for the memory index and memory address counters in the 8-bit and 16-bit instruments.

In trace trigger events with delay not equal to 0, pin 4 of U22 is low. This sets U35C to provide a steady high output, forcing the outputs of U16A and U16C high, regardless of trigger recognition. In this mode, H16STE and H8STE are supplied through U49A and U49B, as controlled by delay gate U21. This circuit holds off counting in the memory address and index counters until the end of the delay period.

In all other modes of operation, U49A and U49B provide steady high states to continuously enable the counters.

SIGNATURE ANALYSIS FOR SCHEMATIC 7B.

The signatures on this schematic are obtained by using DSA Setup A. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. The setup and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A2 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A2, and install A2 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

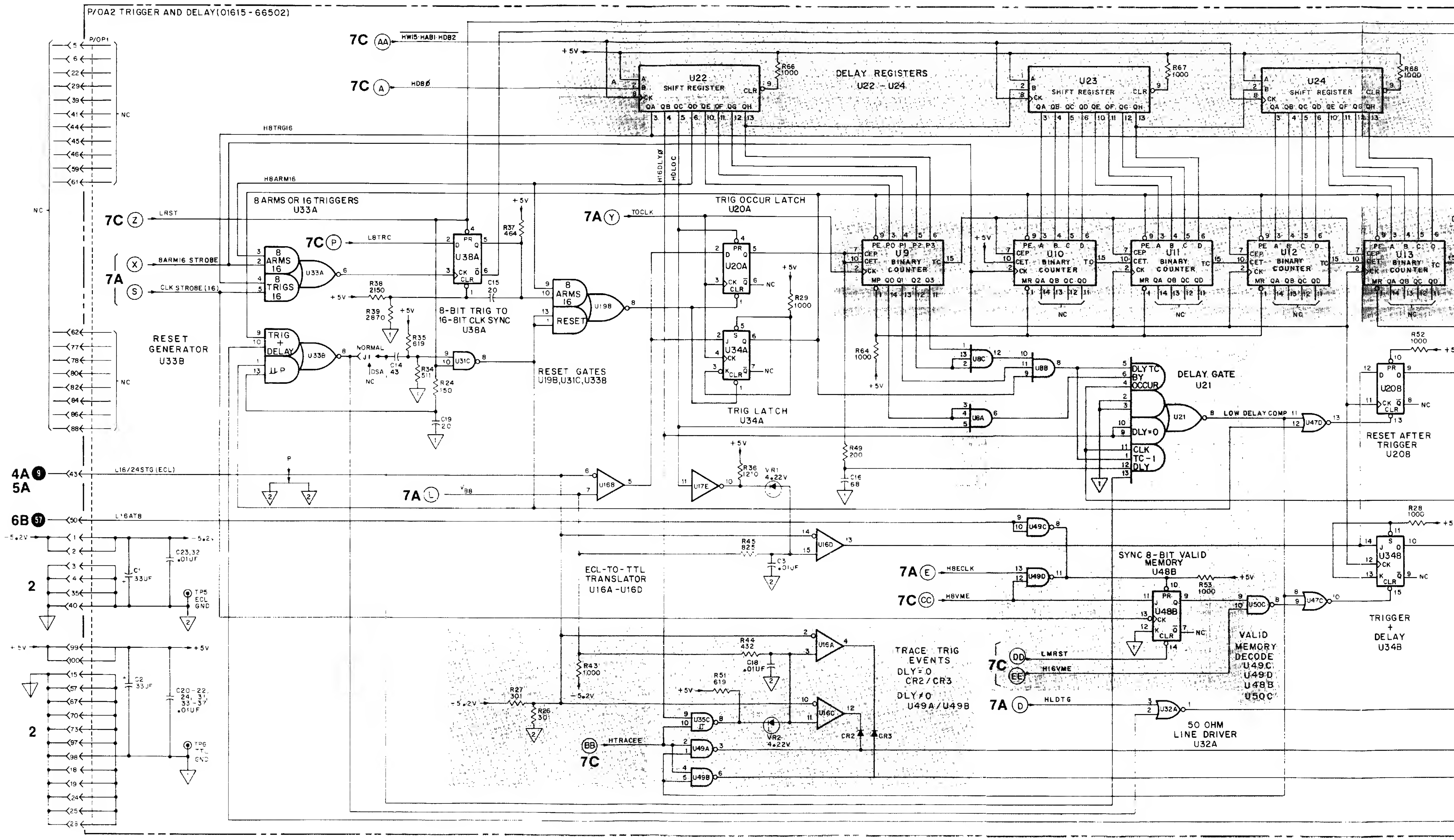
4. Reinstall A5 in 1615A mainframe.

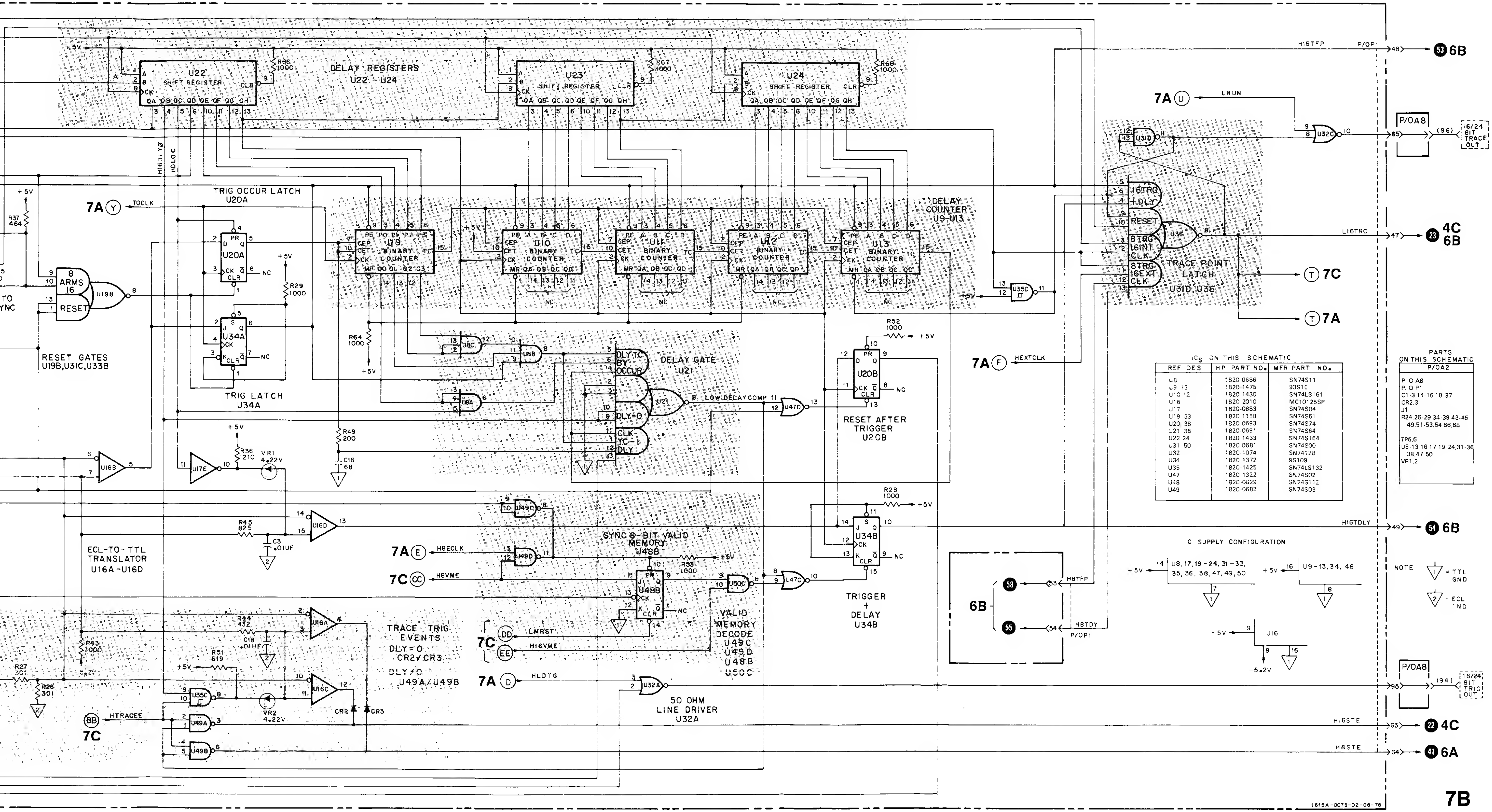
5. Set up signature analyzer as follows:

START ....
STOP ....
CLOCK ....

Signatures for DSA Setup A (Schematic 7B)

Pin	Signature
VH A2U3-14	C690
A2U22-2	FHPA


P/OA2 TRIGGER AND DELAY (01615-66502)
DELAY REGISTERS U22 - U24
8 ARMS OR 16 TRIGGERS U33A
RESET GENERATOR U33B
8-BIT TRIG TO 16-BIT CLK SYNC U38A
RESET GATES U19B,U31C,U33B
TRIG OCCUR LATCH U20A
TRIG LATCH U34A
DELAY GATE U21
RESET AFTER TRIGGER U20B
ECL-TO-TTL TRANSLATOR U16A-U16D
SYNC 8-BIT VALID MEMORY U48B
VALID MEMORY DECODE U49C U49D U48B U50C
TRIGGER + DELAY U34B
TRACE TRIG EVENTS DLY=0 CR2/CR3 DLY≠0 U49A/U49B
50 OHM LINE DRIVER U32A



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U8	1820 0686	SN74S11
U9 13	1820-1475	93S10
U10 12	1820-1430	SN74LS161
U16	1820 2010	MC10125SP
U17	1820-0683	SN74S04
U19 33	1820 1158	SN74S51
U20 38	1820-0693	SN74S74
U21 36	1820-0691	SN74S64
U22 24	1820 1433	SN74S164
U31 50	1820 0681	SN74S00
U32	1820-1074	SN74128
U34	1820 1372	9S109
U35	1820-1425	SN74LS132
U47	1820 1322	SN74S02
U48	1820-0629	SN74S112
U49	1820-0682	SN74S03

PARTS ON THIS SCHEMATIC

P/OA2
P O A8
P. O P1
C1-3 14-16 18 37
CR2,3
J1
R24,26-29 34-39 43-45 49,51-53,64 66,68
TP5,6
U8-13 16 17 19 24,31-36 38,47 50
VR1,2

Figure 8-44.
Trigger and Delay (P/O A2) Schematic

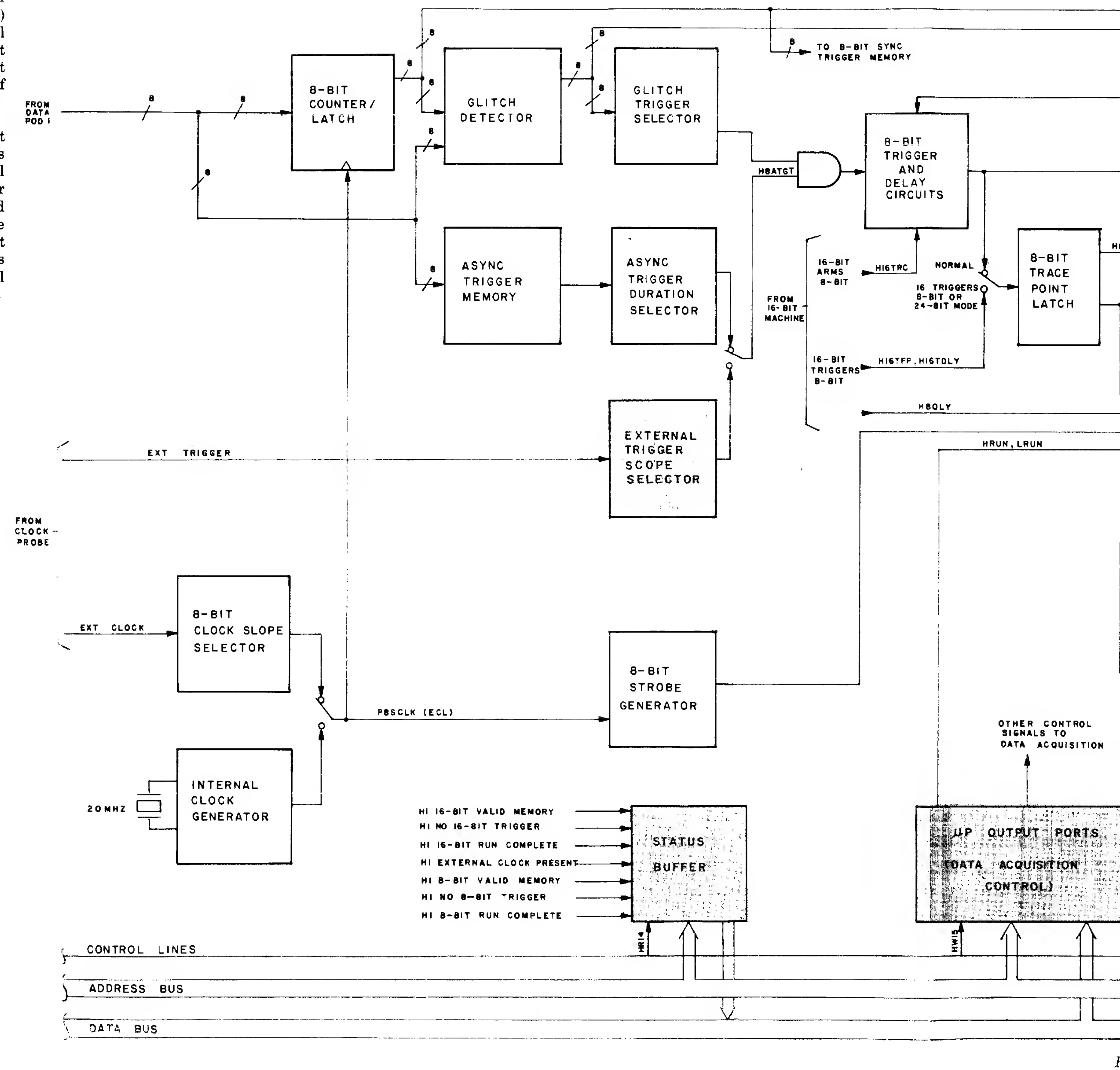
SERVICE SHEET 7C

PRINCIPLES OF OPERATION

U53 is enabled when the microprocessor reads the status of circuits within the 1615A. U25A is used by the microprocessor to latch the trigger and clock specifications for each data-acquisition run.

External Trigger. The external trigger signal from the clock probe is connected through assembly A1 to U41A on assembly A2. U41A supplies the trigger waveform and its complement. The state on pin 19 of U25 determines which slope of the waveform will trigger the 1615A. When pin 19 of U25 is high, U42A is enabled through U43B; this selects the positive edge trigger. When PETRG (ECL) switches high (negative edge switches low), U42B clocks U26A. This sets the $\overline{Q}$ of U26A high. With arrival of the next P8SCLK(ECL) (positive-edge 8-bit sampling clock, ECL), U26B will provide the 8-bit asynchronous trigger condition. At this point, the Q output of U26B sets U26A, returning it to the pretrigger condition. U28A prevents operation of U26B, except when the external trigger is selected.

Slow-clock Detector. When U38B is clocked, its output switches high. When the microprocessor reads status through U53, the high HDB4 is interpreted as a normal condition. After reading the high, the microprocessor clears U38B through HDB5 on U52C. A predetermined time elapses before the microprocessor again reads the output of U38B. If a clock has occurred during that period, HDB4 will again be high. If no clock has occurred, HDB4 will be low and the microprocessor will place the SLOW CLOCK notation on the 1615A CRT.



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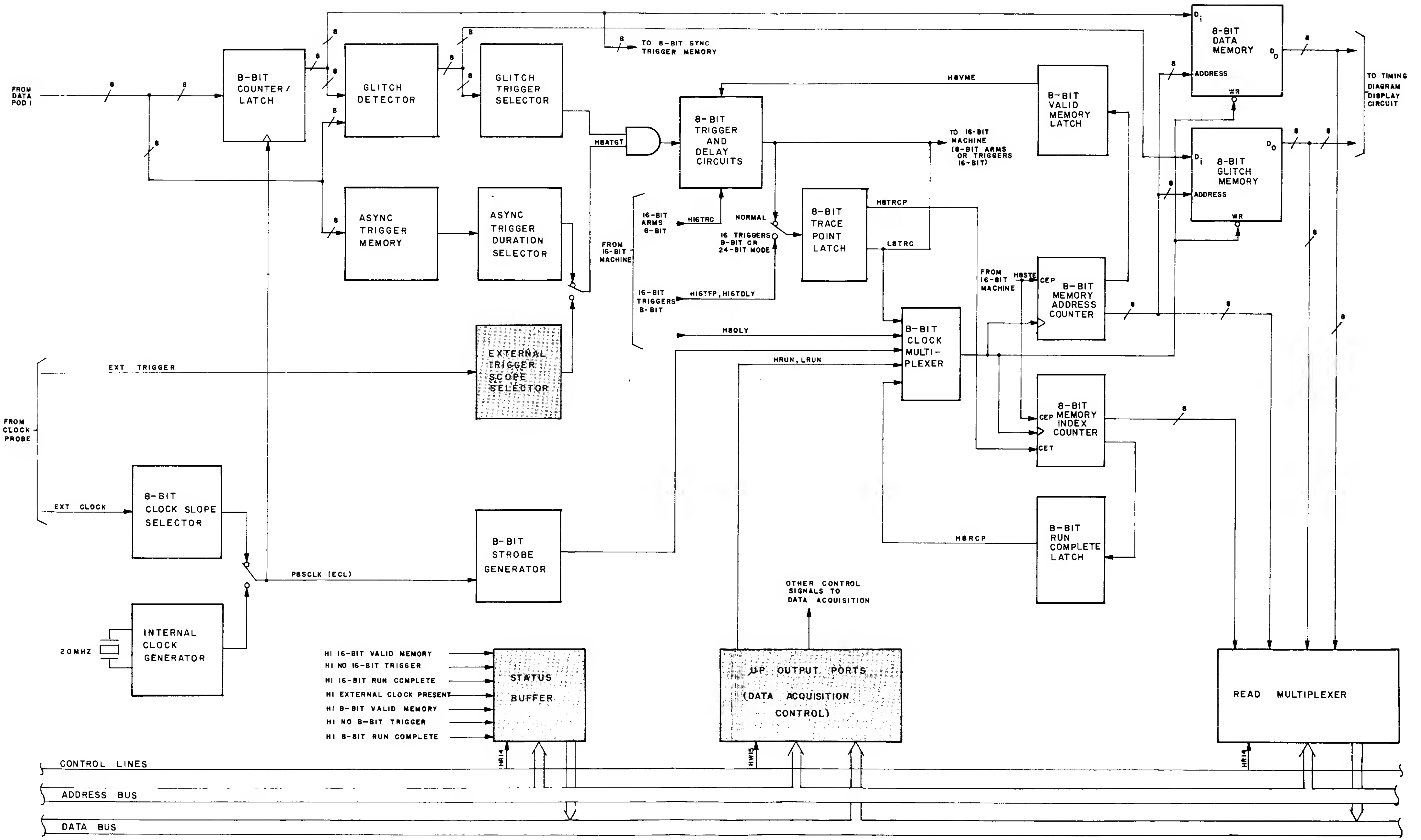


Figure 8-45. Block Diagram, 8-bit Data-acquisition Section for Schematic 7C

SIGNATURE ANALYSIS FOR SCHEMATIC 7C.

The signatures on this schematic are obtained by using DSA Setups A, C, and D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A2 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A2, and install A2 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ↓
STOP .... ↑
CLOCK .... ↓

Signatures for DSA Setup A (Schematic 7C)

Pin	Signature	Pin	Signature
VH A2U3-14	C690	A2U52-9	C6P3
A2U25-3	FHPA	A2U52-13	AHA3
A2U25-4	57CA	A2U53-3	427H
A2U25-7	08F5	A2U53-5	FA2P
A2U25-8	AHA3	A2U53-7	C6P3
A2U25-13	C43H	A2U53-9	C43H
A2U25-14	C6P3	A2U53-12	AHA3
A2U25-17	FA2P	A2U53-14	08F5
A2U25-18	427H	A2U53-16	57CA
A2U50-2	C43H	A2U53-18	FHPA
A2U52-5	08F5		

DSA SETUP C.

1. Remove assembly A2 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A2, and install A2 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   d. Connect signature analyzer stop line to same point as start line, step c above.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 part number is 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... _|¯
STOP.................................... _|¯
CLOCK.................................. ¯|_

Signatures for DSA Setup C (Schematic 7C)

Pin	Signature	Pin	Signature
VH A2U3-14	0001	A2U35-5	4978
A2U35-1	UPFH	A2U35-6	4979
A2U35-2	3827	A2U53-1	4978
A2U35-3	4978	A2U53-19	4979
A2U35-4	4978		

DSA SETUP D.

1. Remove assembly A2 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A2, and install A2 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   c. Connect signature analyzer stop line to same point as start line, step b above.

   d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{WR}$ line.

4. Reinstall A5 in 1615A mainframe.

NOTE

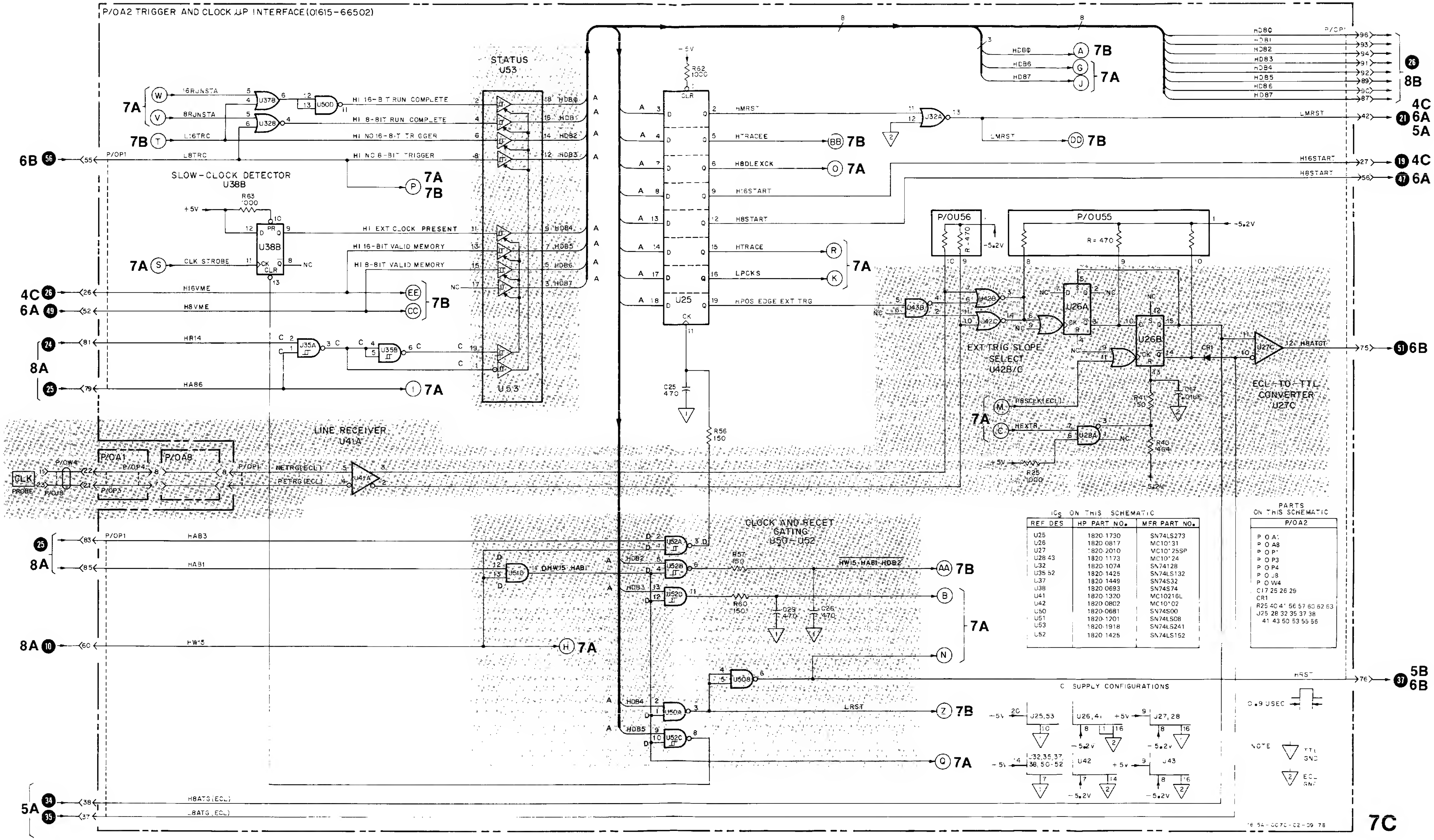
DSA jumper on A5 remains in NM (normal) position in this test setup.

5. Set up signature analyzer as follows:

START .... _|¯
STOP.................................... _|¯
CLOCK.................................. _|¯

Signatures for DSA Setup D (Schematic 7C)

Pin	Signature	Pin	Signature
VH A2U3-14	0001	A2U52-2	7F7H
A2U50-1	9118	A2U52-3	0P51
A2U51-11	9118	A2U52-4	9118
A2U51-12	5554	A2U52-10	9118
A2U51-13	755P	A2U52-12	9118
A2U52-1	755P		



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U25	1820-1730	SN74LS273
U26	1820-0817	MC10131
U27	1820-2010	MC10125SP
U28 43	1820-1173	MC10124
U32	1820-1074	SN74128
U35 52	1820-1425	SN74LS132
U37	1820-1449	SN74S32
U38	1820-0693	SN74S74
U41	1820-1320	MC10216L
U42	1820-0802	MC10102
U50	1820-0681	SN74S00
U51	1820-1201	SN74LS08
U53	1820-1918	SN74LS241
U52	1820-1425	SN74LS152

PARTS ON THIS SCHEMATIC

P/OA2
P/O A1
P/O A8
P/O P1
P/O P3
P/O P4
P/O J8
P/O W4
C17 25 26 29
CR1
R25 40 41 56 57 60 62 63
U25 28 32 35 37 38 41 43 50 53 55 56

Figure 8-46.
Trigger and Clock, Microprocessor Interface (P/O A2) Schematic

SERVICE SHEET 8A

PRINCIPLES OF OPERATION

Timing Generation. The 20-MHz system clock is applied to a divide-by-three network consisting of U14A and U14B. This network generates asymetrical clocks called PDCLK and NDCLK (Positive and Negative Display Clocks). PDCLK is high for 50 ns and low for 100 ns. NDCLK is the inverse of PDCLK.

U15 is wired as a 6-bit shift register, clocked by PDCLK. U16 ANDs the outputs of the first five states of U15 and provides a low to the first stage of the shift register when all of the ANDed outputs are high. Therefore only one bit in the six-bit register is low at any one time. This network divides the clock rate of PDCLK by six.

U26B and RS latches U17A through U17D provide the system timing signals required by the microprocessor and the display processor. U13F and U13C provide the 2-phase nonoverlapping clock for the microprocessor (Φ1 and Φ2).

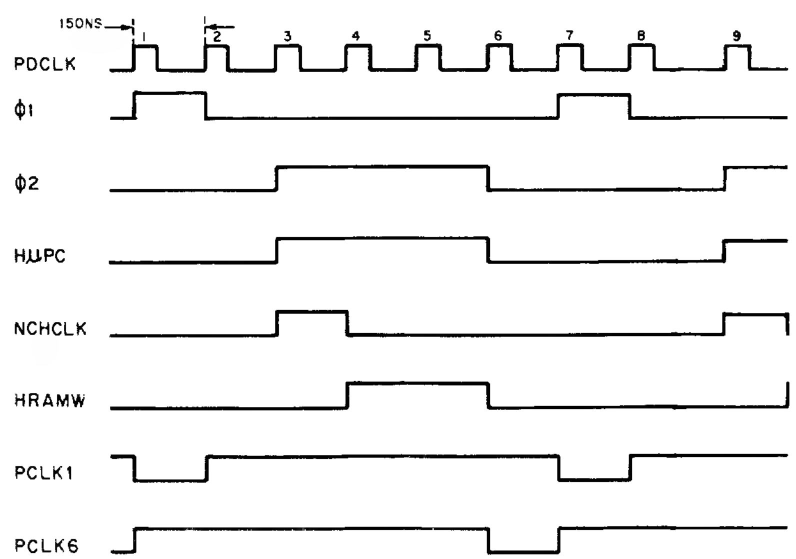
Microprocessor. The 8080A Microprocessor U11 is an N-channel MOS device with a 16-line address bus and an 8-line data bus. It monitors all keyboard switches available to the operator and configures the 1615A circuits according to the selected operating modes and measurements. It also controls all data acquisition and data manipulation in the 1615A. In addition, it provides diagnostic routines for self-test and it generates error and status messages.

Data Bus. The data bus is the only bidirectional bus in the 1615A. During microprocessor read operations, DBIN (U11, pin 17) enables the incoming set of buffers in U12 and U24. This routes all information on the data bus to the microprocessor. During microprocessor write operations, DBIN enables the outgoing set of buffers in U12 and U24. This transfers the data from the microprocessor to the data bus. U25A keeps the buffers in the write mode except when the microprocessor orders a read.

Address Bus. Buffers U10 and U23 increase the drive capability of the microprocessor. The microprocessor address bus selects locations in ROM and RAM, and controls most hardware in the instrument. The first 16K addresses are used for ROM and RAM. The top 1K addresses of this 16K are used for RAM. Addresses above 16K are dedicated to I/O to control the operation of the 1615A.

Microprocessor Read/Write Logic. Information from ROM is available on the data bus when the first 12K of address space is accessed (HAB13 and HAB15 low). HREAD is high, and pins 7 and 9 of U1 are high. U2 enables U25C and HREAD drives U26C low. U9 buffers the selected ROM output. LRAMA (Low RAM Address) enables reading and writing in RAM. HAB14 and HAB15 are used as a linear select to the I/O locations. That is HAB14 is ANDed with HREAD, and HAB15 is ANDed with HWR. Therefore all I/O read instructions use HR14, and all I/O write instructions use HW15, with lower addresses selecting particular locations for each read or write.

Microprocessor Power-up Circuit. C2, R1 through R3, and U26A form the power-up circuit that resets the microprocessor to its start-up routine at instrument turn-on. The voltage across R3 holds the RESET input of the microprocessor high for a time interval determined by RC network C2, R1, and R4. The microprocessor program counter is cleared during this time. When C2 charges sufficiently, U26 sets the microprocessor RESET input low. This releases the microprocessor to start at location 0 in memory.



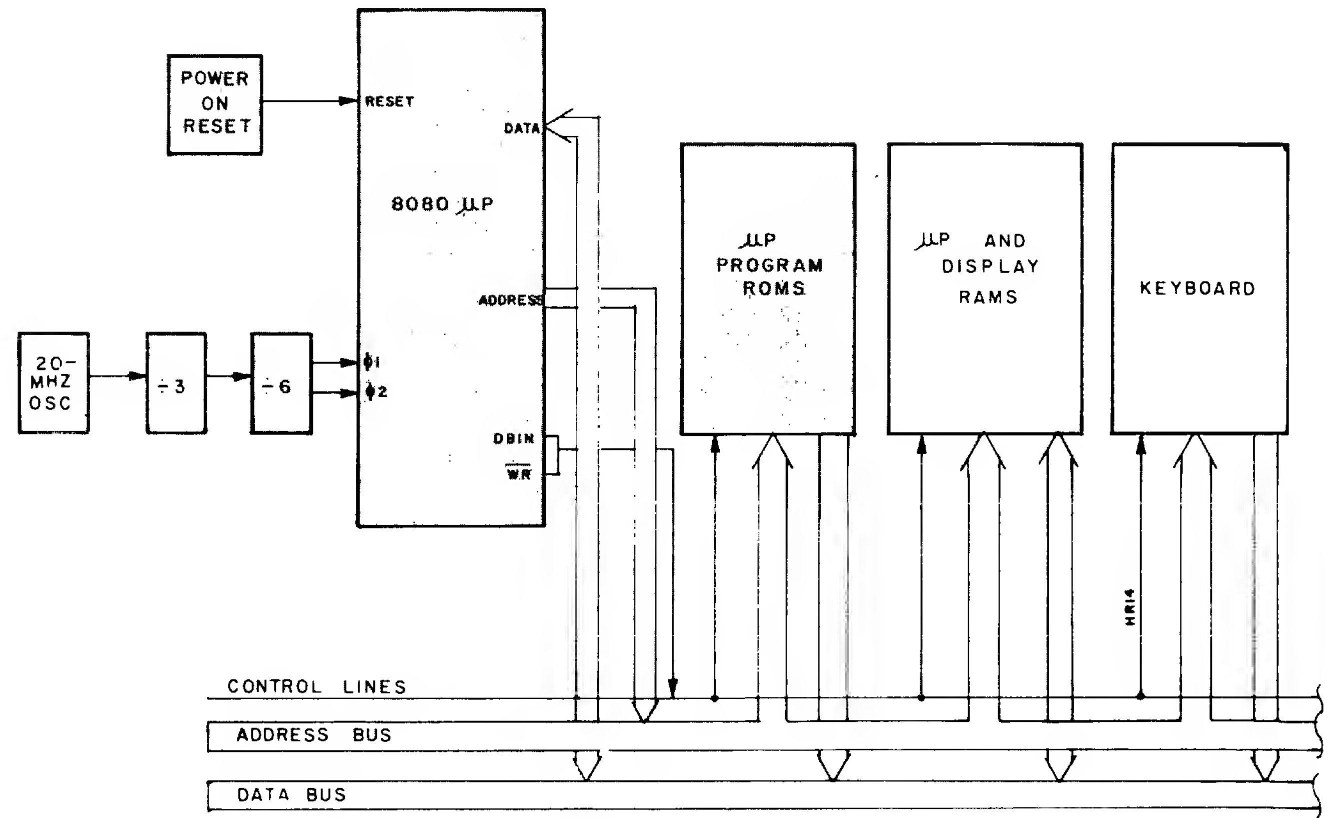


Figure 8-47. Block Diagram, Control Section for Schematic 8A.

SIGNATURE ANALYSIS FOR SCHEMATIC 8A.

The signatures on this schematic are obtained by using DSA Setups A through D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A5 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A5 and install A5 on the extender. Proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 part number is 01615-66505). This is the DBIN line from the microprocessor.

3. Set up signature analyzer as follows:

START .... ⌊
STOP.................................... ⌈
CLOCK.................................. ⌊

Signatures for DSA Setup A (Schematic 8A)

Pin	Signature
VH A5U1-16	C690
A5U2-5*	C690 (blinking)
A5U2-7*	C690 (blinking)
A5U2-9*	C690 (blinking)
A5U2-10*	0548
A5U2-14*	C690 (blinking)
A5U8-9	FHPA
A5U8-10	57CA
A5U8-11	08F5
A5U8-13	AHA3
A5U8-14	C43H
A5U8-15	C6P3
A5U8-16	FA2P
A5U8-17	427H
A5U9-1	0000 (blinking)
A5U9-2	FHPA
A5U9-3	427H
A5U9-4	57CA
A5U9-5	FA2P
A5U9-6	08F5
A5U9-7	C6P3
A5U9-8	AHA3
A5U9-9	C43H
A5U9-11	C43H
A5U9-12	AHA3
A5U9-13	C6P3
A5U9-14	08F5
A5U9-15	FA2P
A5U9-16	57CA
A5U9-17	427H
A5U9-18	FHPA
A5U9-19	C690 (blinking)

*Signatures not for A5 HP Part No. 01615-66505. If checking A5 HP Part No. 01615-66505, A5U2 will have same signatures as A5U8.

DSA SETUP B (B0 THROUGH B6).

1. Remove assembly A5 and the extender board from the 1615A mainframe. Install the extender board in the connector for A5 and install A5 on the extender board. Set up A5 as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall jumper in SA terminals.

   c. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

2. Set up signature analyzer as follows:

START .... ‾|_
STOP .... _|‾
CLOCK .... ‾|_

3. Check part number of A5. If A5 is not 01615-66505, check signatures on A5U2 before checking signatures on any ROM. Proceed as follows:

   a. Connect signature analyzer start and stop lines to A5U8 pin 20 (chip select of ROM 0).

   b. Measure signatures on A5U2 according to table for DSA Setup A5U2.

DSA Setup A5U2 (for A5 not HP Part No. 01615-66505)

Pin	Signature
A5U2-5	7A70 (blinking)
A5U2-7	7A70 (blinking)
A5U2-9	7A70 (blinking)
A5U2-10	8P54
A5U2-14	7A70 (blinking)

4. To perform signature analysis of ROM 0, proceed as follows:

   a. Connect signature analyzer start and stop lines to A5U8 pin 20 (chip select of ROM 0).

   b. Measure signatures of ROM 0 according to the table for DSA Setup B0.

Signatures for DSA Setup B0 (Schematic 8A)

Pin	Signature
VH A5U1-16	7A70
A5U8-9	9UAF
A5U8-10	UAH0
A5U8-11	PF1P
A5U8-13	32F7
A5U8-14	HU39
A5U8-15	U0A6
A5U8-16	0AA9
A5U8-17	60H2
A5U9-1	0000 (blinking)
A5U9-2	9UAF
A5U9-3	60H2
A5U9-4	UAH0
A5U9-5	0AA9
A5U9-6	PF1P
A5U9-7	U0A6
A5U9-8	32F7
A5U9-9	HU39
A5U9-11	HU39
A5U9-12	32F7
A5U9-13	U0A6
A5U9-14	PF1P
A5U9-15	0AA9
A5U9-16	UAH0
A5U9-17	60H2
A5U9-18	9UAF
A5U9-19	7A70 (blinking)

5. To perform signature analysis of ROM 1, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U7 pin 20 (chip select of ROM 1).

b. Measure signatures of ROM 1 according to the table for DSA Setup B1.

Signatures for DSA Setup B1 (Schematic 8A)

Pin	Signature
VH A5U1-16	7A70
A5U7-9	U6H4
A5U7-10	20CU
A5U7-11	72U2
A5U7-13	2563
A5U7-14	HF06
A5U7-15	AFPH
A5U7-16	9753
A5U7-17	F97P
A5U9-1	0000 (blinking)
A5U9-2	U6U4
A5U9-3	F97P
A5U9-4	20CU
A5U9-5	9753
A5U9-6	72U2
A5U9-7	AFPH
A5U9-8	2563
A5U9-9	HF06
A5U9-11	HF06
A5U9-12	2563
A5U9-13	AFPH
A5U9-14	72U2
A5U9-15	9753
A5U9-16	20CU
A5U9-17	F97P
A5U9-18	U6H4
A5U9-19	7A70 (blinking)

6. To perform signature analysis of ROM 2, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U6 pin 20 (chip select of ROM 2).

b. Measure signatures of ROM 2 according to the table for DSA Setup B2.

Signatures for DSA Setup B2 (Schematic 8A)

Pin	Signature
VH A5U1-16	7A70
A5U6-9	29UF
A5U6-10	0758
A5U6-11	F434
A5U6-13	U59A
A5U6-14	U55C
A5U6-15	774F
A5U6-16	CUC6
A5U6-17	FFUH
A5U9-1	0000 (blinking)
A5U9-2	29UF
A5U9-3	FFUH
A5U9-4	0758
A5U9-5	CUC6
A5U9-6	F434
A5U9-7	774F
A5U9-8	U59A
A5U9-9	U55C
A5U9-11	U55C
A5U9-12	U59A
A5U9-13	774F
A5U9-14	F434
A5U9-15	CUC6
A5U9-16	0758
A5U9-17	FFUH
A5U9-18	29UF
A5U9-19	7A70 (blinking)

7. To perform signature analysis of ROM 3, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U5 pin 20 (chip select of ROM 3).

b. Measure signatures of ROM 3 according to the table for DSA Setup B3.

Signatures for DSA Setup B3 (Schematic 8A)

Pin	Signature
VH A5U1-16	7A70
A5U5-9	81CC
A5U5-10	UH2P
A5U5-11	CU43
A5U5-13	59P8
A5U5-14	9912
A5U5-15	6U16
A5U5-16	A732
A5U5-17	HCP8
A5U9-1	0000 (blinking)
A5U9-2	81CC
A5U9-3	HCP8
A5U9-4	UH2P
A5U9-5	A732
A5U9-6	CU43
A5U9-7	6U16
A5U9-8	59P8
A5U9-9	9912
A5U9-11	9912
A5U9-12	59P8
A5U9-13	6U16
A5U9-14	CU43
A5U9-15	A732
A5U9-16	UH2P
A5U9-17	HCP8
A5U9-18	81CC
A5U9-19	7A70 (blinking)

8. To perform signature analysis of ROM 4, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U4 pin 20 (chip select of ROM 4).

b. Measure signatures of ROM 4 according to the table for DSA Setup B4.

Signatures for DSA Setup B4 (Schematic 8A)

Pin	Signature
VH A5U1-16	7A70
A5U4-9	2135
A5U4-10	0572
A5U4-11	8FPP
A5U4-13	7HU0
A5U4-14	0HF4
A5U4-15	8957
A5U4-16	A8F5
A5U4-17	4P43
A5U9-1	0000 (blinking)
A5U9-2	2135
A5U9-3	4P43
A5U9-4	0572
A5U9-5	A5F5
A5U9-6	85PP
A5U9-7	8957
A5U9-8	7HU0
A5U9-9	0HF4
A5U9-11	0HF4
A5U9-12	7HU0
A5U9-13	8957
A5U9-14	85PP
A5U9-15	A5F5
A5U9-16	0572
A5U9-17	4P43
A5U9-18	2135
A5U9-19	7A70 (blinking)

9. To perform signature analysis of ROM 5, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U3 pin 20 (chip select of ROM 5).

b. Measure signatures of ROM 5 according to the table for DSA Setup B5.

Signatures for DSA Setup B5 (Schematic 8A)

Pin	Signature
VH A5U1-16	7A70
A5U3-9	UPUH
A5U3-10	C92C
A5U3-11	5087
A5U3-13	PC9P
A5U3-14	7PH2
A5U3-15	610A
A5U3-16	A740
A5U3-17	F4FH
A5U9-1	0000 (blinking)
A5U9-2	UPUH
A5U9-3	F4FH
A5U9-4	C92C
A5U9-5	A740
A5U9-6	5087
A5U9-7	610A
A5U9-8	PC9P
A5U9-9	7PH2
A5U9-11	7PH2
A5U9-12	PC9P
A5U9-13	610A
A5U9-14	5087
A5U9-15	A740
A5U9-16	C92C
A5U9-17	F4FH
A5U9-18	UPUH
A5U9-19	7A70 (blinking)

10. To perform signature analysis of ROM 6, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U2 pin 20 (chip select of ROM 6).

b. Measure signatures of ROM 6 according to the table for DSA Setup B6.

Signatures for DSA Setup B6 (A5 Part No. 01615-66505 only)

Pin	Signature
VH A5U1-16	7A70
A5U2-9	0486
A5U2-10	4525
A5U2-11	F125
A5U2-13	6431
A5U2-14	1250
A5U2-15	040F
A5U2-16	FA71
A5U2-17	FP53
A5U9-1	0000 (blinking)
A5U9-2	0486
A5U9-3	FP53
A5U9-4	4525
A5U9-5	FA71
A5U9-6	F125
A5U9-7	040F
A5U9-8	6431
A5U9-9	1250
A5U9-11	1250
A5U9-12	6431
A5U9-13	040F
A5U9-14	F125
A5U9-15	FA71
A5U9-16	4525
A5U9-17	FP53
A5U9-18	0486
A5U9-19	7A70 (blinking)

DSA SETUP C.

1. Remove assembly A5 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A5 and install A5 on the extender. Proceed as follows:

a. Remove A5U12 and A5U24.

b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall jumper in the SA terminals.

c. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 is part number 01615-66505). This is the address bit A15.

d. Connect signature analyzer stop line to same point as start line, step c above.

e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

2. Set up signature analyzer as follows:

START ....
STOP ....
CLOCK ....

Signatures for DSA Setup C (Schematic 8A)

Pin	Signature if A5 is Part No.:	
	not 01615-66505	01615-66505
VH A5U1-16	0001	0001
A5U1-1	1293	1293
A5U1-2	HAP7	HAP7
A5U1-3	3C96	3C96
A5U1-4	755P	755P
A5U1-5	3827	3827
A5U1-6	0001	0001
A5U1-7	1920	1920
A5U1-9	C34C	C34C
A5U1-10	597C	597C
A5U1-11	UA87	UA87
A5U1-12	4154	4154
A5U1-13	960F	960F
A5U1-14	84AF	84AF
A5U1-15	3PCF	3PCF
A5U2-5	C34C	——
A5U2-7	AA6A	——
A5U2-9	2AU9	——
A5U2-10	HPP0	——
A5U2-14	1920	——
A5U8-1	52F8	52F8
A5U8-2	UPFH	UPFH
A5U8-3	0AFA	0AFA
A5U8-4	5H21	5H21

Signatures for DSA Setup C (Schematic 8A) (Cont'd)

Pin	Signature if A5 is Part No.:	
	not 01615-66505	01615-66505
A5U8-5	7F7F	7F7F
A5U8-6	CCCC	CCCC
A5U8-7	5555	5555
A5U8-8	UUUU	UUUU
A5U8-9	FA44	FA44
A5U8-10	1825	1825
A5U8-11	31A0	31A0
A5U8-13	0209	0209
A5U8-14	8200	8200
A5U8-15	H1A1	H1A1
A5U8-16	0U96	0U96
A5U8-17	P16U	P16U
A5U8-19	HPP0	HPP0
A5U8-20	3PCF	3PCE
A5U8-22	2H70	2H70
A5U8-23	HC89	HC89
A5U2-20	——	C34C
A5U3-20	597C	597C
A5U4-20	UA87	UA87
A5U5-20	4154	4154
A5U6-20	960F	960F
A5U7-20	84AF	84AF
A5U9-1	FPC5	7HUU
A5U9-2	FA44	FA44
A5U9-4	1825	1825
A5U9-6	31A0	31A0
A5U9-8	0209	0209
A5U9-11	8200	8200
A5U9-13	H1A1	H1A1
A5U9-15	0U96	0U96
A5U9-17	P16U	P16U
A5U9-19	FPC4	7HUP
A5U10-2	HPP0	HPP0
A5U10-3	3827	3827
A5U10-4	1293	1293
A5U10-5	HAP7	HAP7
A5U10-6	3C96	3C96
A5U10-7	755P	755P
A5U10-8	2H70	2H70
A5U10-9	HC89	HC89
A5U10-11	HC89	HC89
A5U10-12	2H70	2H70
A5U10-13	755P	755P
A5U10-14	3C96	3C96
A5U10-15	HAP7	HAP7
A5U10-16	1293	1293
A5U10-17	3827	3827
A5U10-18	HPP0	HPP0
A5U10-19	0001	0001
A5U11-1	HPP0	HPP0
A5U11-12	0000	0000
A5U11-17	0001 (blinking)	0001 (blinking)
A5U11-20	0001	0001
A5U11-23	0001	0001
A5U11-25	UUUU	UUUU
A5U11-26	5555	5555

Signatures for DSA Setup C (Schematic 8A) (Cont'd)

Pin	Signature if A5 is Part No.: not 01615-66505	01615-66505
A5U11-27	CCCC	CCCC
A5U11-29	7F7F	7F7F
A5U11-30	5H21	5H21
A5U11-31	0AFA	0AFA
A5U11-32	UPFH	UPFH
A5U11-33	52F8	52F8
A5U11-34	HC89	HC89
A5U11-35	2H70	2H70
A5U11-36	755P	755P
A5U11-37	HAP7	HAP7
A5U11-38	3C96	3C96
A5U11-39	3827	3827
A5U11-40	1293	1293
A5U12-1	0001 (blinking)	0001 (blinking)
A5U12-13	0001 (blinking)	0001 (blinking)
A5U13-1	755P	755P
A5U13-2	64HU	64HU
A5U13-3	FPC5	7HUU
A5U13-4	FPC4	7HUP
A5U13-10	64HU	64HU
A5U13-11	3827	3827
A5U23-2	UUUU	UUUU
A5U23-3	52F8	52F8
A5U23-4	5555	5555
A5U23-5	UPFH	UPFH
A5U23-6	CCCC	CCCC
A5U23-7	0AFA	0AFA
A5U23-8	7F7F	7F7F
A5U23-9	5H21	5H21
A5U23-11	5H21	5H21
A5U23-12	7F7F	7F7F
A5U23-13	0AFA	0AFA
A5U23-14	CCCC	CCCC
A5U23-15	UPFH	UPFH
A5U23-16	5555	5555
A5U23-17	52F8	52F8
A5U23-18	UUUU	UUUU
A5U23-19	0001	0001
A5U24-1	0001 (blinking)	0001 (blinking)
A5U24-13	0001 (blinking)	0001 (blinking)
A5U25-1	0001	0001
A5U25-2	0001 (blinking)	0001 (blinking)
A5U25-3	0001 (blinking)	0001 (blinking)
A5U25-4	0000	0000
A5U25-5	755P	755P
A5U25-6	0000	0000
A5U25-8	FPC4	7HUP
A5U25-9	64HU	64HU
A5U25-10	AA6A	1920
A5U25-11	3827	3827
A5U25-12	3827	3827
A5U25-13	0001 (blinking)	0001 (blinking)
A5U26-1	0001	0001
A5U26-2	0001	0001
A5U26-3	0000	0000
A5U26-8	FPC5	7HUU
A5U26-9	FPC4	7HUP
A5U26-10	0001 (blinking)	0001 (blinking)

DSA SETUP D.

1. Remove assembly A5 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A5 and install A5 on the extender. Proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   c. Connect signature analyzer stop line to same point as start line, step b above.

   d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{WR}$ line.

NOTE

DSA jumper on A5 remains in NM (normal) position in this DSA setup.

3. Set up signature analyzer as follows:

START ....

STOP ....

CLOCK ....

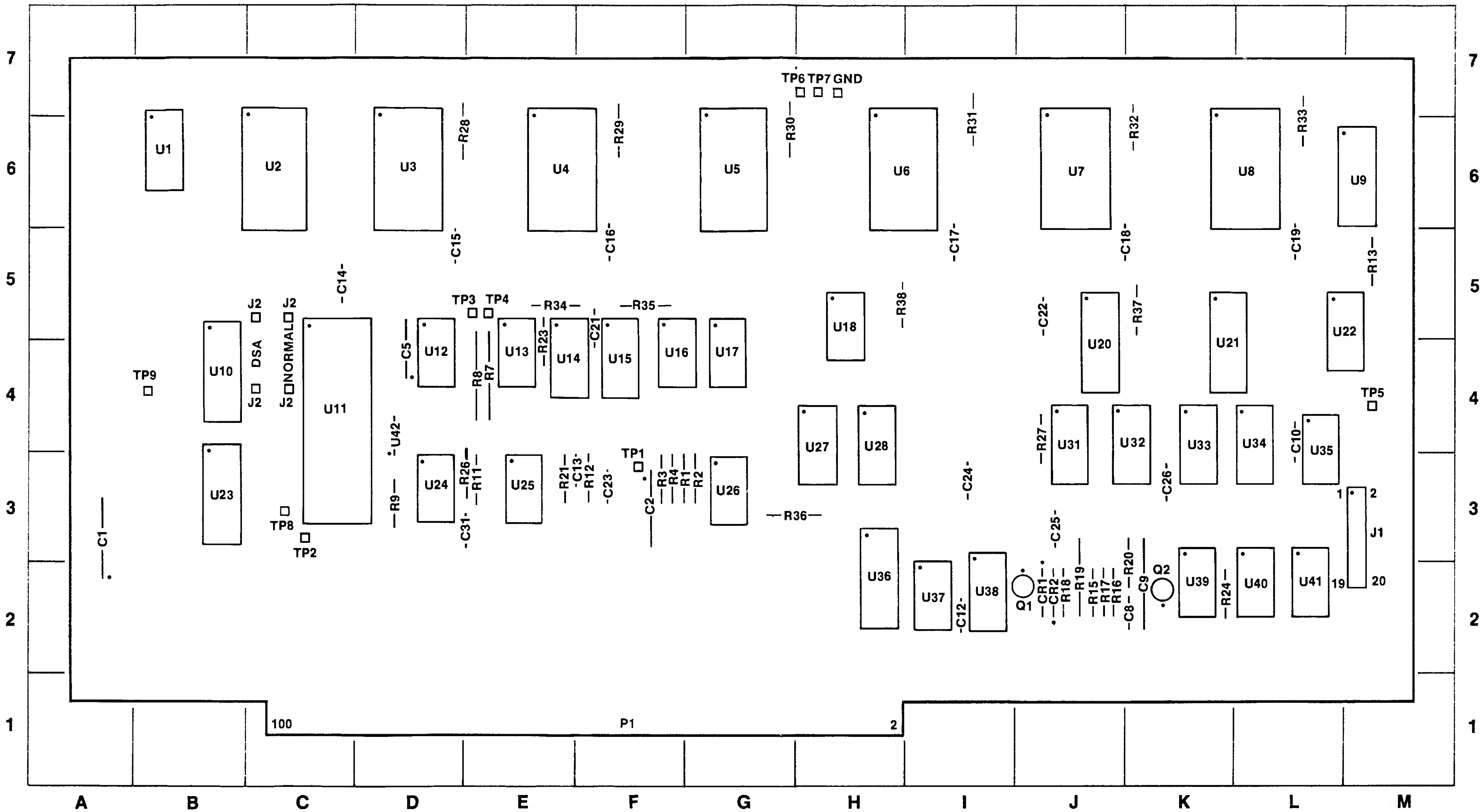
Signatures for DSA Setup D (Schematic 8A)

Pin	Signature
VH A5U1-16	0001
A5U1-1	1292
A5U1-2	HAP6
A5U1-3	3C97
A5U1-4	755P
A5U1-5	3826
A5U1-6	0001
A5U1-7	71H4
A5U1-9	H6F4
A5U1-10	7807
A5U1-11	2FF3
A5U1-12	PF2P
A5U1-13	8F14
A5U1-14	U81U
A5U1-15	7A71
A5U2-5*	H6F4
A5U2-7*	A711
A5U2-9*	U121
A5U2-10*	HPP1
A5U2-14*	71H4
A5U10-2	HPP1
A5U10-3	3826
A5U10-4	1292
A5U10-5	HAP6
A5U10-6	3C97
A5U10-7	755P

*Do not measure on A5 Part No. 01615-66505.

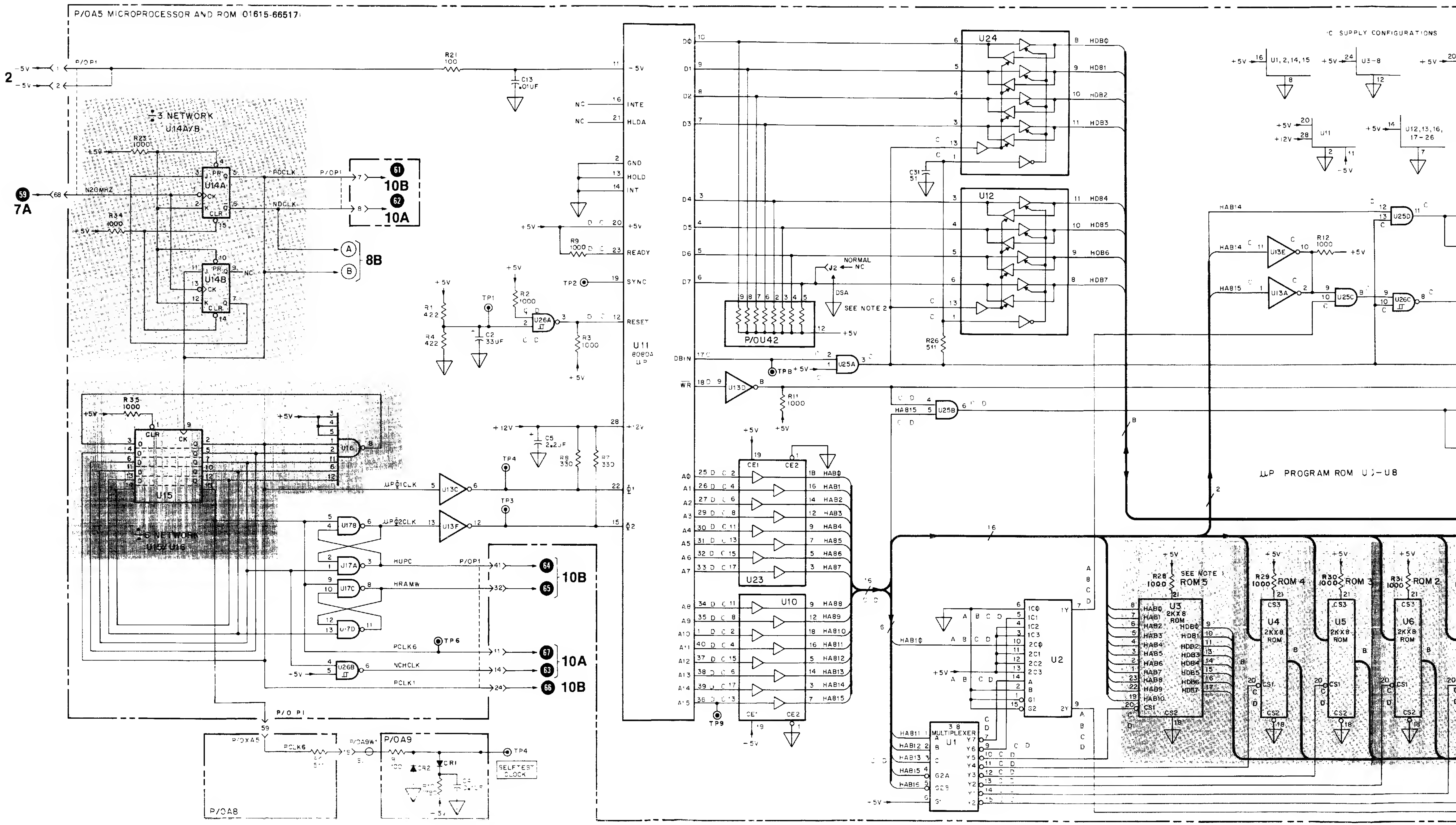
Signatures for DSA Setup D (Schematic 8A) (Cont'd)

Pin	Signature
A5U10-8	2H71
A5U10-9	HC88
A5U10-11	HC88
A5U10-12	2H71
A5U10-13	755P
A5U10-14	3C97
A5U10-15	HAP6
A5U10-16	1292
A5U10-17	3826
A5U10-18	HPP1
A5U10-19	0001
A5U11-1	HPP1
A5U11-12	0000
A5U11-18	0000 (blinking)
A5U11-20	0001
A5U11-23	0001
A5U11-25	UUUP
A5U11-26	5554
A5U11-27	CCCA
A5U11-29	7F7H
A5U11-30	5H20
A5U11-31	0AFC
A5U11-32	UPFF
A5U11-33	52FP
A5U11-34	HC88
A5U11-35	2H71
A5U11-36	755P
A5U11-37	HAP6
A5U11-38	3C97
A5U11-39	3826
A5U11-40	1292
A5U13-8	0001 (blinking)
A5U13-9	0000 (blinking)
A5U23-2	UUUP
A5U23-3	52F9
A5U23-4	5554
A5U23-5	UPFF
A5U23-6	CCCA
A5U23-7	0AFC
A5U23-8	7F7H
A5U23-9	5H20
A5U23-11	5H20
A5U23-12	7F7H
A5U23-13	0AFC
A5U23-14	CCCA
A5U23-15	UPFF
A5U23-16	5554
A5U23-17	52F9
A5U23-18	UUUP
A5U23-19	0001
A5U25-4	0001 (blinking)
A5U25-5	755P
A5U25-6	755P
A5U26-1	0001
A5U26-2	0001
A5U26-3	0000



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	A-3	C17	I-5	CR2	J-2	R9	D-3	R23	E-4	R35	F-5	TP8	C-3	U10	B-4	U21	K-4	U33	K-4
C2	F-3	C18	J-5	J1	M-3	R11	E-3	R24	K-2	R36	G-3	TP9	B-4	U11	C-4	U22	M-5	U34	L-4
C5	D-4	C19	L-5	P1	F-1	R12	F-3	R26	E-3	R37	K-5	U1	B-6	U12	D-4	U23	B-3	U35	L-4
C8	K-2	C21	F-5	Q1	J-2	R13	M-5	R27	J-4	R38	H-5	U2	C-6	U13	E-4	U24	D-3	U36	H-2
C9	K-2	C22	J-5	Q2	K-2	R15	J-2	R28	D-6	TP1	F-3	U3	D-6	U14	E-4	U25	E-3	U37	I-2
C10	L-4	C23	F-3	R1	F-3	R16	J-2	R29	F-6	TP2	C-3	U4	E-6	U15	F-4	U26	G-3	U38	I-2
C12	I-2	C24	I-3	R2	G-3	R17	J-2	R30	G-6	TP3	E-5	U5	G-6	U16	F-4	U27	H-4	U39	K-2
C13	F-3	C25	J-3	R3	F-3	R18	J-2	R31	I-6	TP4	E-5	U6	H-6	U17	G-4	U28	H-4	U40	L-2
C14	C-5	C26	K-3	R4	F-3	R19	J-2	R32	K-6	TP5	M-4	U7	J-6	U18	H-5	U31	J-4	U41	L-2
C15	D-5	C31	E-3	R7	E-4	R20	K-2	R33	L-6	TP6	H-7	U8	L-6	U20	J-4	U32	K-4	U42	D-4
C16	F-5	CR1	J-2	R8	E-4	R21	E-3	R34	E-5	TP7	H-7	U9	M-6						

Figure 8-48. Microprocessor and ROM Assembly A5, Parts Identification


P/OA5 MICROPROCESSOR AND ROM 01615-66517
IC SUPPLY CONFIGURATIONS
µP PROGRAM ROM U3-U8
U11 8080A µP
U24
U12
U23
U10
U2
U1 3-8 MULTIPLEXER
U3 2K X 8 ROM
ROM 5
ROM 4
ROM 3
ROM 2
U4
U5
U6
U14A
U14B
U15
U16
3 NETWORK U14A/B
5 NETWORK U15/U16
P/OU42
SEE NOTE 2
SEE NOTE 1
NORMAL
DSA
SELF TEST CLOCK
P/OA8
P/OA9
10B
10A
8B
7A
2

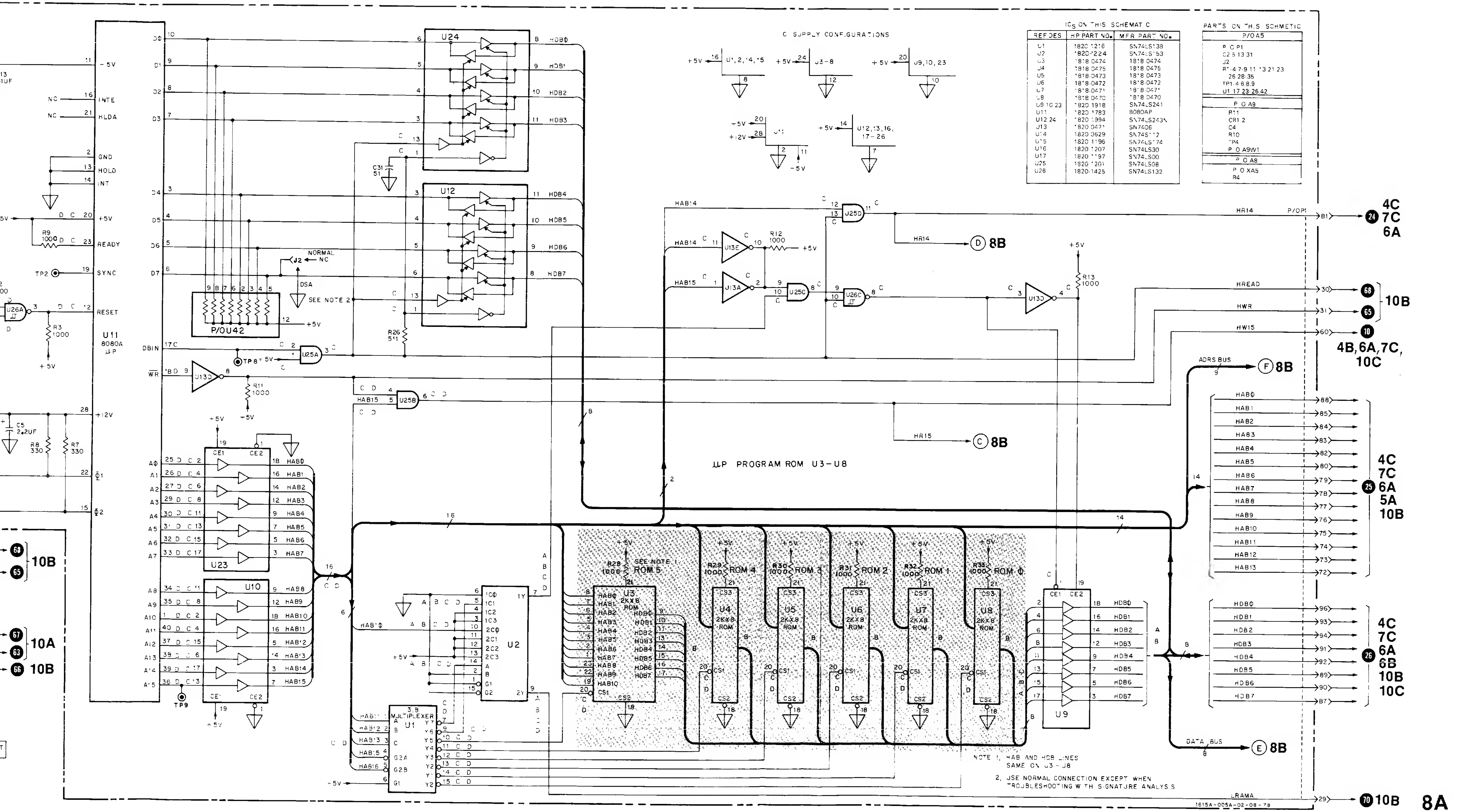


Figure 8-49.
Microprocessor and ROM (P/O A5) Schematic

SERVICE SHEET 8B

PRINCIPLES OF OPERATION

Keyboard Pulse and Control. In the quiescent state, Q1 and Q2 are cut off. U35A is low. U22 is nonconducting. To read the keyboard, the microprocessor forces pin 6 of U35B low. This activates Q1 and Q2 to generate a 90-milliampere pulse on the collector of Q2 which is applied to the keyboard. R17 and C8 control the turn-on of Q2. The low from U35B also activates U22 to place the four lines of data from the keyboard on the data bus.

The keys on the keyboard are divided into a matrix of ten columns of switches with four switches in each column. HAB0 through HAB3 are BCD coded to select one of the ten columns on the keyboard. The 90-milliampere pulse is connected through the four switches in the selected column. Each of the four switches drives a separate output line (HROW0 through HROW3). With no key down, little coupling occurs between the pulse and the output lines. If a key is down, the associated output line (HROW0 through HROW3) receives the current pulse. The microprocessor reads the output lines through U22. The exact key down is detected by decoding HAB0 through HAB3 and HROW0 through HROW3.

When the microprocessor reads a key down, it sets HKYD (High Key Down) high through U40A, U41B, and RS latch U35C and U35D. This changes the threshold, increasing the readability of the down key. HKYD is held high until the microprocessor reads all keys up. They it resets HKYD low again and searches for a new key down.

Trigger Line. U33 and U34 are used during timing diagram presentation. They made up the counter that generates the tic marks showing the location of the trigger word. U21 receives a count signifying the location of TC-COUNT, the trigger word in memory. This count is parallel loaded into U33 and U34 while the 1615A is presenting the channel number. The counter begins its count when display of the timing waveform starts. When the location of the trigger word is reached (terminal count), U34 generates HTLIN (a 150-ns pulse) which paints the trigger tic mark.

Expand Indicator. The expand indicator intensifies a 24-dot segment of a timing diagram during unexpanded displays. The 24-dot segment is the area that will be displayed on screen during expanded (X10) displays. U20 is loaded with a binary count signifying the location of the first dot in the expanded segment. The count in U20 is parallel loaded into U31 and U32 when the 1615A displays the channel number in a timing diagram.

U28 and U27 are normally in the terminal count state. Their high output is inverted through U18C to produce a low HEXPI (High Expand Indicator).

When the 1615A begins displaying the timing waveform, U31 and U32 count the display locations. When U32 reaches terminal count, U28 and U27 are parallel loaded to terminal count minus 24. They count 24 clocks and return to terminal count. During this 24-clock period, HEXPI is high, brightening the 24-dot segment on screen.

Memory Dump and Control. Gate U39 supplies clocks to the 8-bit memory when the 1615A is displaying a timing diagram. The top AND gate in U39 is only active during retrace in magnified displays. During X10 retrace, PDCLK clocks U39 while LMACLD (Low Memory Address Counter Load) parallel loads the address of the starting point of display. After retrace, HHB2 switches low, disabling the gate.

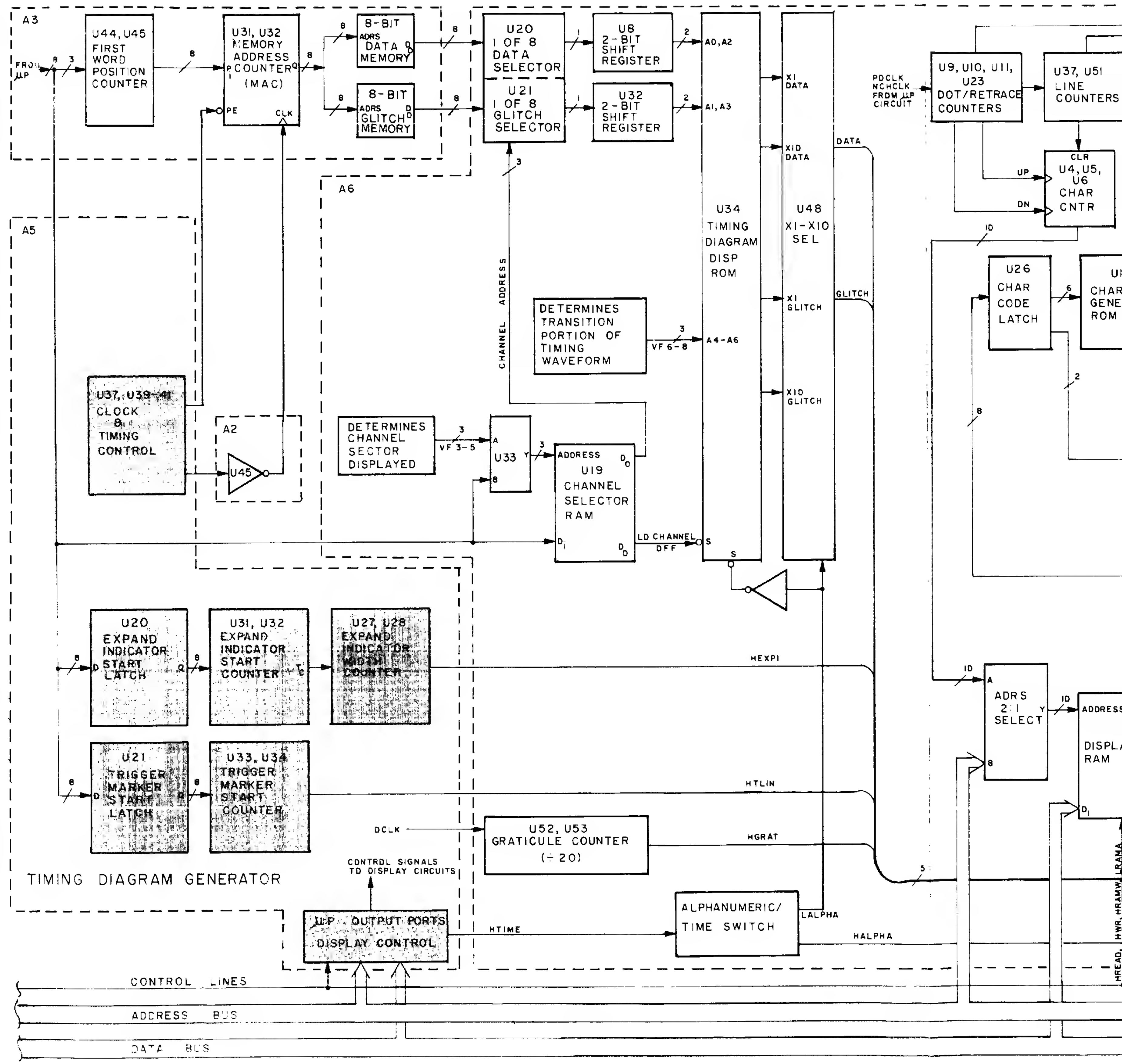
The next AND gate in U39 receives LSTD (Low Start Display) from the microprocessor. LSTD is low only when presenting a timing diagram. At all other times, LSTD is high, preventing clock generation.

The third AND portion of U39 generates clocks to read the data in memory during X1 display magnification.

The fourth AND portion of U39 generates memory-read clocks in X10 display. One of its inputs is decade counter U38 which permits only one out of every ten PDCLK clocks to reach the 8-bit memory address counters. This provides the divide-by-ten function for magnification.

U40B operates only during X10 display magnification. It generates LGLS (Low Glitch Set) one time for every ten PDCLK clocks. LGLS enables glitch display. U40B prevents displaying the same glitch more than one time on an expanded timing diagram.

Display Control. U36 interfaces several channels from the microprocessor that are used in establishing the display mode. U41A, along with U37C and U37D supply LMACLD (Low Memory Address Counter Load). It parallel loads the 8-bit memory address counter with the location of the first data bit to be displayed when showing a timing diagram. LMACLD is generated in timing diagram modes at the beginning of each raster line when 1615A presents a channel number. HSTD and LHB3 are used to disable LMACLD during a memory write or after horizontal retrace blanking.



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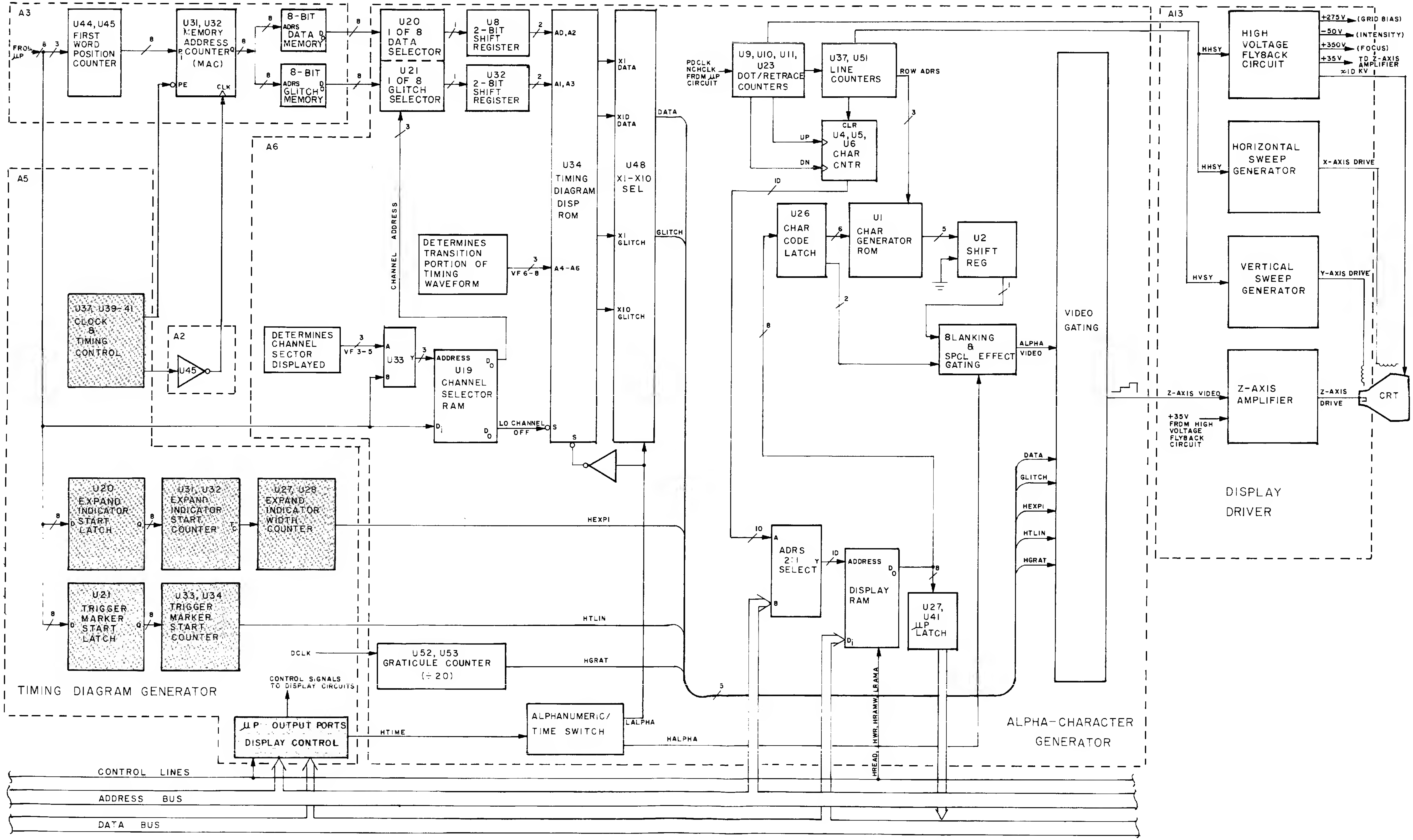


Figure 8-50. Block Diagram, Display Section for Schematic 8B

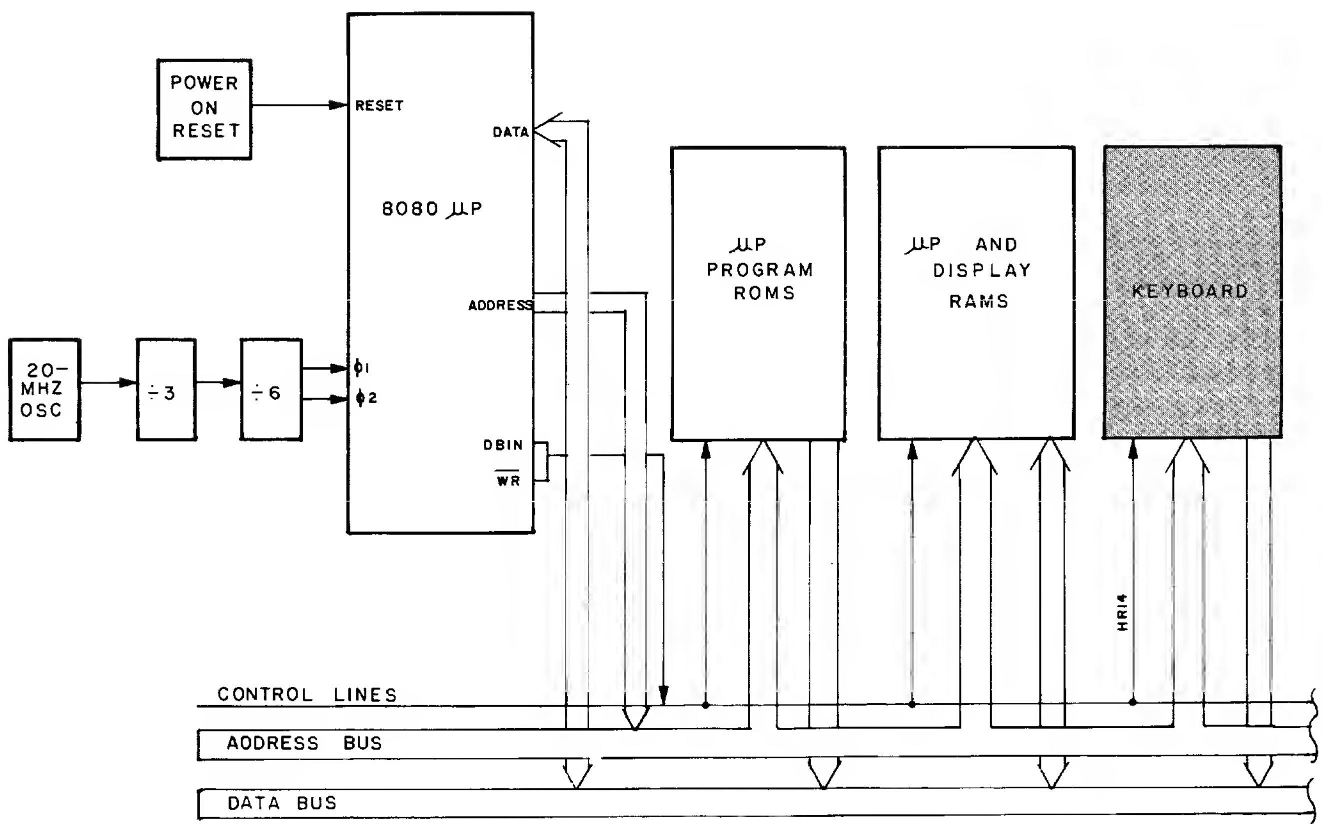


Figure 8-51. Block Diagram, Control Section for Schematic 8B

SIGNATURE ANALYSIS FOR SCHEMATIC 8B.

The signatures on this schematic are obtained by using DSA Setups A through D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A5 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A5 and install A5 on the extender board. Proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

3. Set up signature analyzer as follows:

START .... ʅ
STOP.................................... ʃ
CLOCK.................................. ʅ

Signatures for DSA Setup A (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	C690	A5U21-18	FHPA
A5U20-3	427H	A5U22-3	FHPA
A5U20-4	FA2P	A5U22-5	57CA
A5U20-7	C6P3	A5U22-7	08F5
A5U20-8	C6P3	A5U22-9	AHA3
A5U20-13	AHA3	A5U36-3	FHPA
A5U20-14	08F5	A5U36-4	57CA
A5U20-17	57CA	A5U36-7	08F5
A5U20-18	FHPA	A5U36-8	AHA3
A5U21-3	427H	A5U36-13	C43H
A5U21-4	FA2P	A5U36-14	C6P3
A5U21-7	C693	A5U36-17	FA2P
A5U21-8	C43H	A5U36-18	427H
A5U21-13	AHA3	A5U40-2	C6P3
A5U21-14	08F5	A5U41-13	C43H
A5U21-17	57CA		

DSA SETUP B (B0 THROUGH B6).

1. Remove assembly A5 and the extender board from the 1615A mainframe. Install the extender board in the connector for A5 and install A5 on the extender board. Set up A5 as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall jumper in SA terminals.

   c. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

2. Set up signature analyzer as follows:

START .... ʅ
STOP.................................... ʃ
CLOCK.................................. ʅ

3. To perform signature analysis of ROM 0 effects on components shown on schematic 8B, proceed as follows:

   a. Connect signature analyzer start and stop lines to A5U8 pin 20 (chip select of ROM 0).

   b. Measure signatures of ROM 0 according to the table for DSA Setup B0.

Signatures for DSA Setup B0 (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	7A70	A5U21-18	9UAF
A5U20-3	60H2	A5U22-3	9UAF
A5U20-4	0AA9	A5U22-5	UAH0
A5U20-7	U0A6	A5U22-7	PF1P
A5U20-8	HU39	A5U22-9	32F7
A5U20-13	32F7	A5U36-3	9UAF
A5U20-14	PF1P	A5U36-4	UAH0
A5U20-17	UAH0	A5U36-7	PF1P
A5U20-18	9UAF	A5U36-8	32F7
A5U21-3	60H2	A5U36-13	HU39
A5U21-4	0AA9	A5U36-14	U0A6
A5U21-7	U0A6	A5U36-17	0AA9
A5U21-8	HU39	A5U36-18	60H2
A5U21-13	32F7	A5U40-2	U0A6
A5U21-14	PF1P	A5U41-13	HU39
A5U21-17	UAH0		

4. To perform signature analysis of ROM 1 effects on components shown on schematic 8B, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U7 pin 20 (chip select of ROM 1).

b. Measure signatures of ROM 1 according to the table for DSA Setup B1.

Signatures for DSA Setup B1 (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	7A70	A5U21-18	U6H4
A5U20-3	F97P	A5U22-3	U6H4
A5U20-4	9753	A5U22-5	20CU
A5U20-7	AFPH	A5U22-7	72U2
A5U20-8	HF06	A5U22-9	2563
A5U20-13	2563	A5U36-3	U6H4
A5U20-14	72U2	A5U36-4	20CU
A5U20-17	20CU	A5U36-7	72U2
A5U20-18	U6H4	A5U36-8	2563
A5U21-3	F97P	A5U36-13	HF06
A5U21-4	9753	A5U36-14	AFPH
A5U21-7	AFPH	A5U36-17	9753
A5U21-8	HF06	A5U36-18	F97P
A5U21-13	2563	A5U40-2	AFPH
A5U21-14	72U2	A5U41-13	HF06
A5U21-17	20CU		

5. To perform signature analysis of ROM 2 effects on components shown on schematic 8B, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U6 pin 20 (chip select of ROM 2).

b. Measure signatures of ROM 2 according to the table for DSA Setup B2.

Signatures for DSA Setup B2 (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	7A70	A5U21-18	29UF
A5U20-3	FFUH	A5U22-3	29UF
A5U20-4	CUC6	A5U22-5	0758
A5U20-7	774F	A5U22-7	F434
A5U20-8	U55C	A5U22-9	U59A
A5U20-13	U59A	A5U36-3	29UF
A5U20-14	F434	A5U36-4	0758
A5U20-17	0758	A5U36-7	F434
A5U20-18	29UF	A5U36-8	U59A
A5U21-3	FFUH	A5U36-13	U55C
A5U21-4	CUC6	A5U36-14	774F
A5U21-7	774F	A5U36-17	CUC6
A5U21-8	U55C	A5U36-18	FFUH
A5U21-13	U59A	A5U40-2	774F
A5U21-14	F434	A5U41-13	U55C
A5U21-17	0758		

6. To perform signature analysis of ROM 3 effects on components shown on schematic 8B, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U5 pin 20 (chip select of ROM 3).

b. Measure signatures of ROM 3 according to the table for DSA Setup B3.

Signatures for DSA Setup B3 (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	7A70	A5U21-18	81CC
A5U20-3	HCP8	A5U22-3	81CC
A5U20-4	A732	A5U22-5	UH2P
A5U20-7	6U16	A5U22-7	CU43
A5U20-8	9912	A5U22-9	59P8
A5U20-13	59P8	A5U36-3	81CC
A5U20-14	CU43	A5U36-4	UH2P
A5U20-17	UH2P	A5U36-7	CU43
A5U20-18	81CC	A5U36-8	59P8
A5U21-3	HCP8	A5U36-13	9912
A5U21-4	A732	A5U36-14	6U16
A5U21-7	6U16	A5U36-17	A732
A5U21-8	9912	A5U36-18	HCP8
A5U21-13	59P8	A5U40-2	6U16
A5U21-14	CU43	A5U41-13	9912
A5U21-17	UF2P		

7. To perform signature analysis of ROM 4 effects on components shown on schematic 8B, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U4 pin 20 (chip select of ROM 4).

b. Measure signatures of ROM 4 according to the table for DSA Setup B4.

Signatures for DSA Setup B4 (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	7A70	A5U21-18	2135
A5U20-3	4P43	A5U22-3	2135
A5U20-4	A5F5	A5U22-5	0572
A5U20-7	8957	A5U22-7	8FPP
A5U20-8	0HF4	A5U22-9	7HU0
A5U20-13	7HU0	A5U36-3	2135
A5U20-14	8FPP	A5U36-4	0572
A5U20-17	0572	A5U36-7	8FPP
A5U20-18	2135	A5U36-8	7HU0
A5U21-3	4P43	A5U36-13	0HF4
A5U21-4	A5F5	A5U36-14	8957
A5U21-7	8957	A5U36-17	85F5
A5U21-8	0HF4	A5U36-18	4P43
A5U21-13	7HU0	A5U40-2	8957
A5U21-14	8FPP	A5U41-13	0HF4
A5U21-17	0572		

8. To perform signature analysis of ROM 5 effects on components shown on schematic 8B, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U3 pin 20 (chip select of ROM 5).

b. Measure signatures of ROM 5 according to the table for DSA Setup B5.

Signatures for DSA Setup B5 (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	7A70	A5U21-18	UPUH
A5U20-3	F4FH	A5U22-3	UPUH
A5U20-4	A740	A5U22-5	C92C
A5U20-7	610A	A5U22-7	5087
A5U20-8	7PH2	A5U22-9	PC9P
A5U20-13	PC9P	A5U36-3	UPUH
A5U20-14	5087	A5U36-4	C92C
A5U20-17	C92C	A5U36-7	5087
A5U20-18	UPUH	A5U36-8	PC9P
A5U21-3	F4FH	A5U36-13	7PH2
A5U21-4	A740	A5U36-14	610A
A5U21-7	610A	A5U36-17	A740
A5U21-8	7PH2	A5U36-18	F4FH
A5U21-13	PC9P	A5U40-2	610A
A5U21-14	5087	A5U41-13	7PH2
A5U21-17	C92C		

9. To perform signature analysis of ROM 6 effects on components shown on schematic 8B, proceed as follows:

a. Connect signature analyzer start and stop lines to A5U2 pin 20 (chip select of ROM 6).

b. Measure signatures of ROM 6 according to the table for DSA Setup B6.

Signatures for DSA Setup B6 (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	7A70	A5U21-18	0486
A5U20-3	FP53	A5U22-3	0486
A5U20-4	FA71	A5U22-5	4525
A5U20-7	040F	A5U22-7	F125
A5U20-8	1250	A5U22-9	6431
A5U20-13	6431	A5U36-3	0486
A5U20-14	F125	A5U36-4	4525
A5U20-17	4525	A5U36-7	F125
A5U20-18	0486	A5U36-8	6431
A5U21-3	FP53	A5U36-13	1250
A5U21-4	FA71	A5U36-14	040F
A5U21-7	040F	A5U36-17	FA71
A5U21-8	1250	A5U36-18	FP53
A5U21-13	6431	A5U40-2	040F
A5U21-14	F125	A5U41-13	1250
A5U21-17	4525		

DSA SETUP C.

1. Remove assembly A5 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A5 and install A5 on the extender board. Proceed as follows:

a. Remove A5U12 and A5U24.

b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

c. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is the address bit A15.

d. Connect signature analyzer stop line to same point as start line, step c above.

e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 part number is 01615-66505). This is the DBIN line from the microprocessor.

3. Set up signature analyzer as follows:

START .... ↑
STOP.................................... ↑
CLOCK.................................. ↓

Signatures for DSA Setup C (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U1-16	0001	A5U35-4	HC89
A5U35-1	0001	A5U35-5	3827
A5U35-2	HP5A	A5U35-6	HP5A
A5U35-3	HP5C		

DSA SETUP D.

1. Remove assembly A5 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A5 and install A5 on the extender board. Proceed as follows:

a. Remove A5U12 and A5U24.

b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

c. Connect signature analyzer stop line to same point as start line, step b above.

d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{WR}$ line.

NOTE

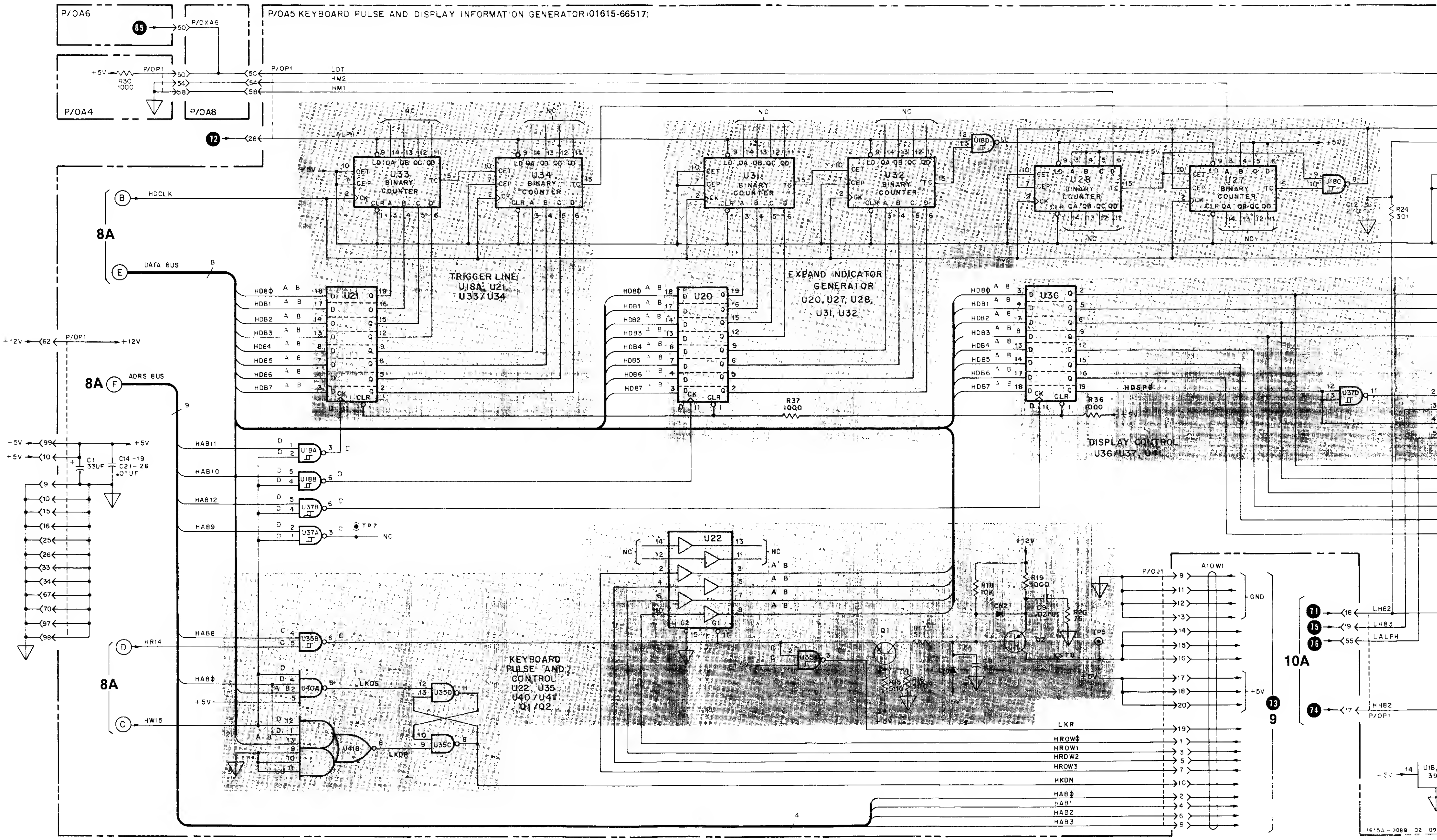
DSA jumper on A5 remains in NM (normal) position in this DSA setup.

3. Set up signature analyzer as follows:

START .... ↑
STOP.................................... ↑
CLOCK.................................. ↑

Signatures for DSA Setup D (Schematic 8B)

Pin	Signature	Pin	Signature
VH A5U16-1	0001	A5U37-1	755P
A5U18-1	1292	A5U37-2	2H71
A5U18-2	755P	A5U37-3	0U55
A5U18-3	PP0H	A5U37-4	755P
A5U18-4	755P	A5U37-5	HAP6
A5U18-5	HPP1	A5U37-6	0421
A5U18-6	7639	A5U40-1	755P
A5U20-11	7639	A5U40-4	UUUP
A5U21-11	PP0H	A5U41-1	UUUP
A5U36-11	0421	A5U41-12	755P


P/OA5 KEYBOARD PULSE AND DISPLAY INFORMATION GENERATOR (01615-66517)
P/OA6
P/OA4
P/OA8
TRIGGER LINE
U18A, U21,
U33/U34
EXPAND INDICATOR
GENERATOR
U20, U27, U28,
U31, U32
DISPLAY CONTROL
U36/U37/U41
KEYBOARD
PULSE AND
CONTROL
U22, U35
U40/U41
Q1/Q2
BINARY COUNTER
DATA BUS
ADRS BUS
HDCLK
8A
10A
9

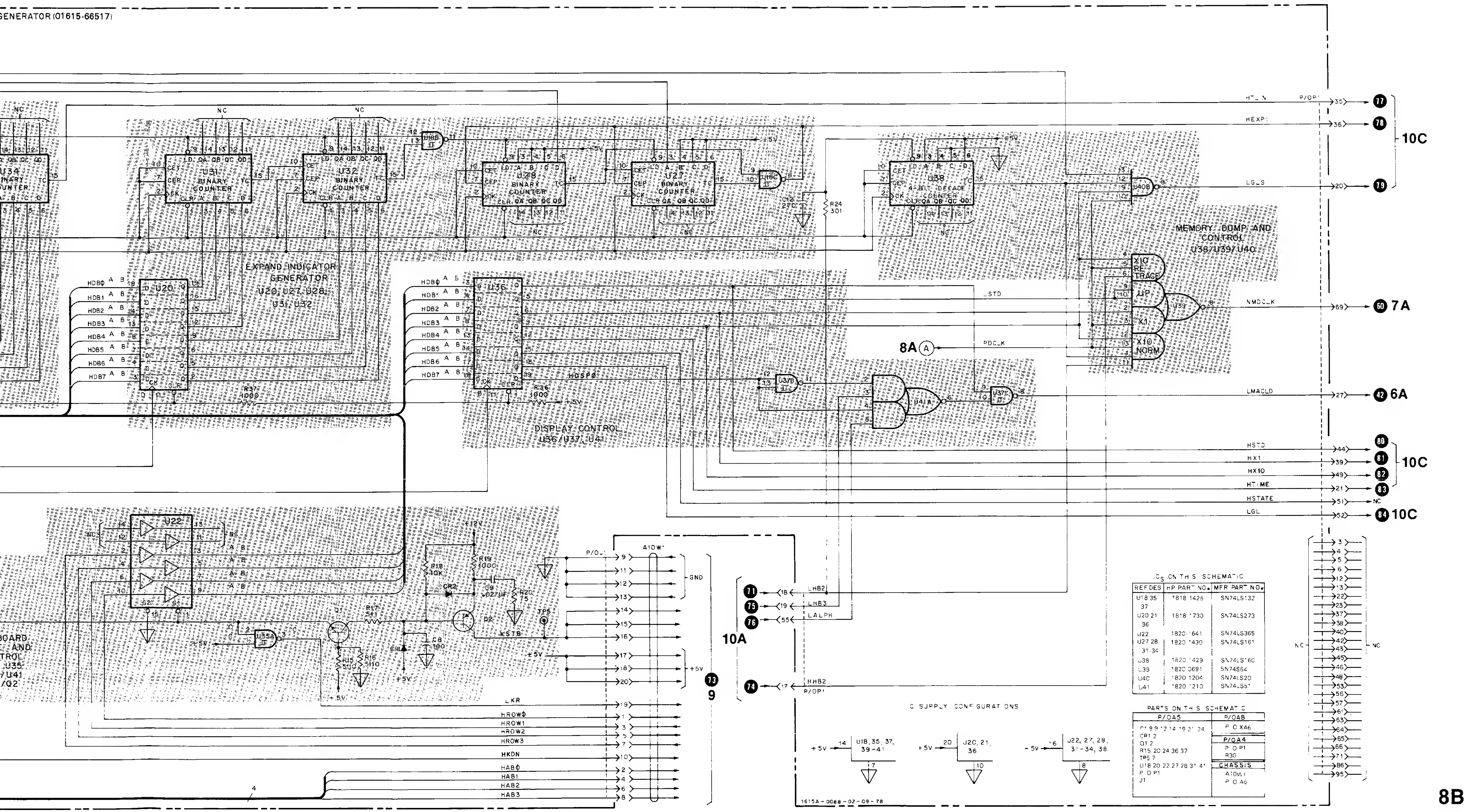


Figure 8-52.
Keyboard Pulse and Display Information Generators (P/O A5) Schematic

SERVICE SHEET 9

PRINCIPLES OF OPERATION

Key Switches. The key switches are wired in a matrix of ten columns by four rows. Each switch has two 1-turn coils wrapped around a core. When a key is relaxed (not pressed), a magnet within the switch is positioned so that its field saturates the core. The saturated core permits very little coupling between coils. When the key is pressed, the magnet is moved out of the core, allowing the core and windings to act as a transformer.

Key Sensing. A 4-bit byte from the microprocessor (HAB0 through HAB3) is decoded by BCD-to-decimal decoder U1. This grounds one column of switches, allowing the other nine columns to float. HKBR is a 90-milliampere pulse from the keyboard control on assembly A5. It is applied to the switch column that is grounded through U1. Then the 4-bit byte is incremented and U1 grounds the next column in sequence.

If a key is down in the column grounded by U1, flux is coupled from the primary to the secondary windings in the key switch. This activates the associated output integrator (U3B through U3E), causing it to produce a negative-going output pulse.

A low output from any integrator sets the associated RS latch high. When the microprocessor detects a high from any latch (key down), it determines the key position by decoding the row indicated and the internal column count (4-bit byte). LKR (Low Key Reset) is a clock that continuously resets the RS latches.

When the microprocessor detects a key down, it sets HKYD (High Key Down) high. This offsets the bias point of integrators U3B through U3E. The result of the bias shift is a translation downward of the quiescent output level of U3B through U3E. Now less total flux is required to maintain the negative-going integrator output pulse. The additional hysterisis introduced by HKYD prevents multiple readings of key switch entries. When all keys are read in the up position for one scan, HKYD is returned low.

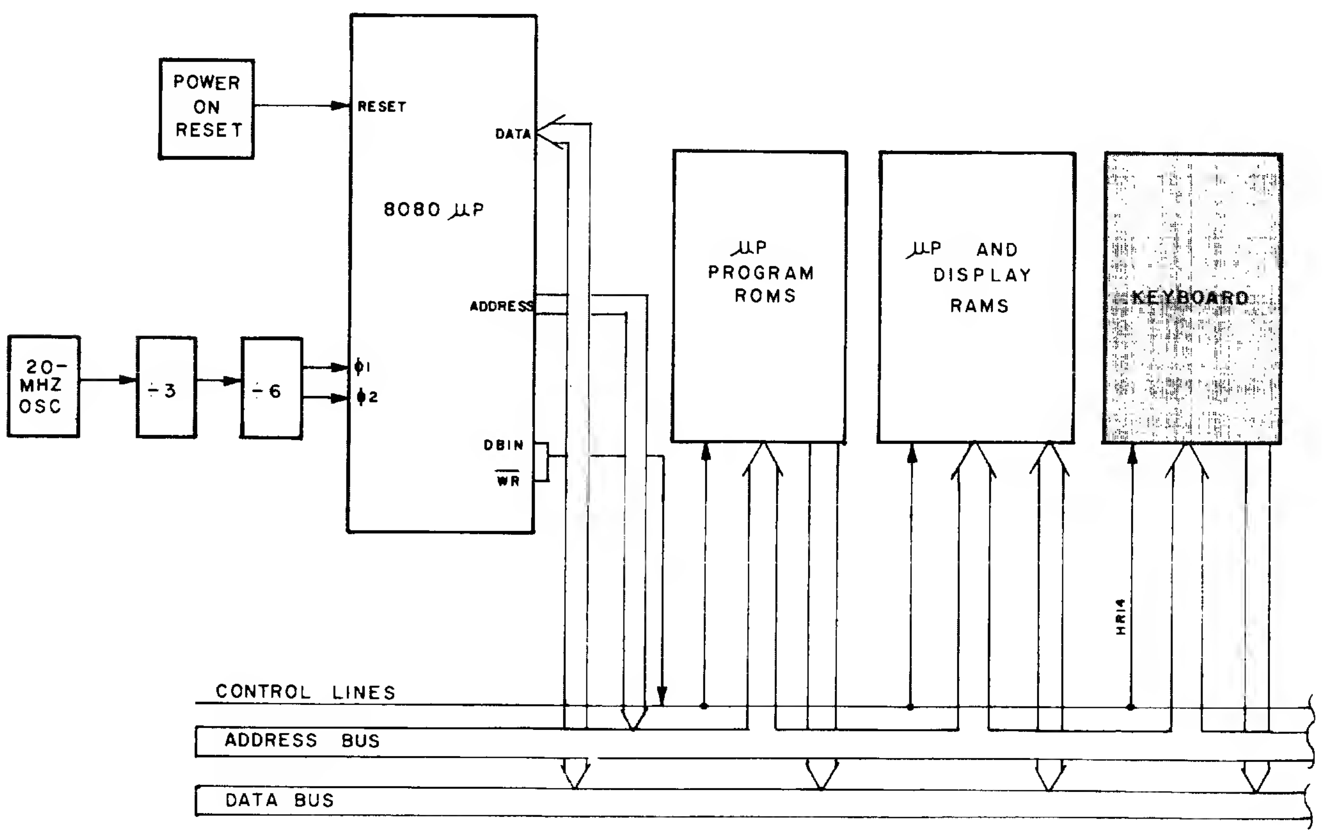
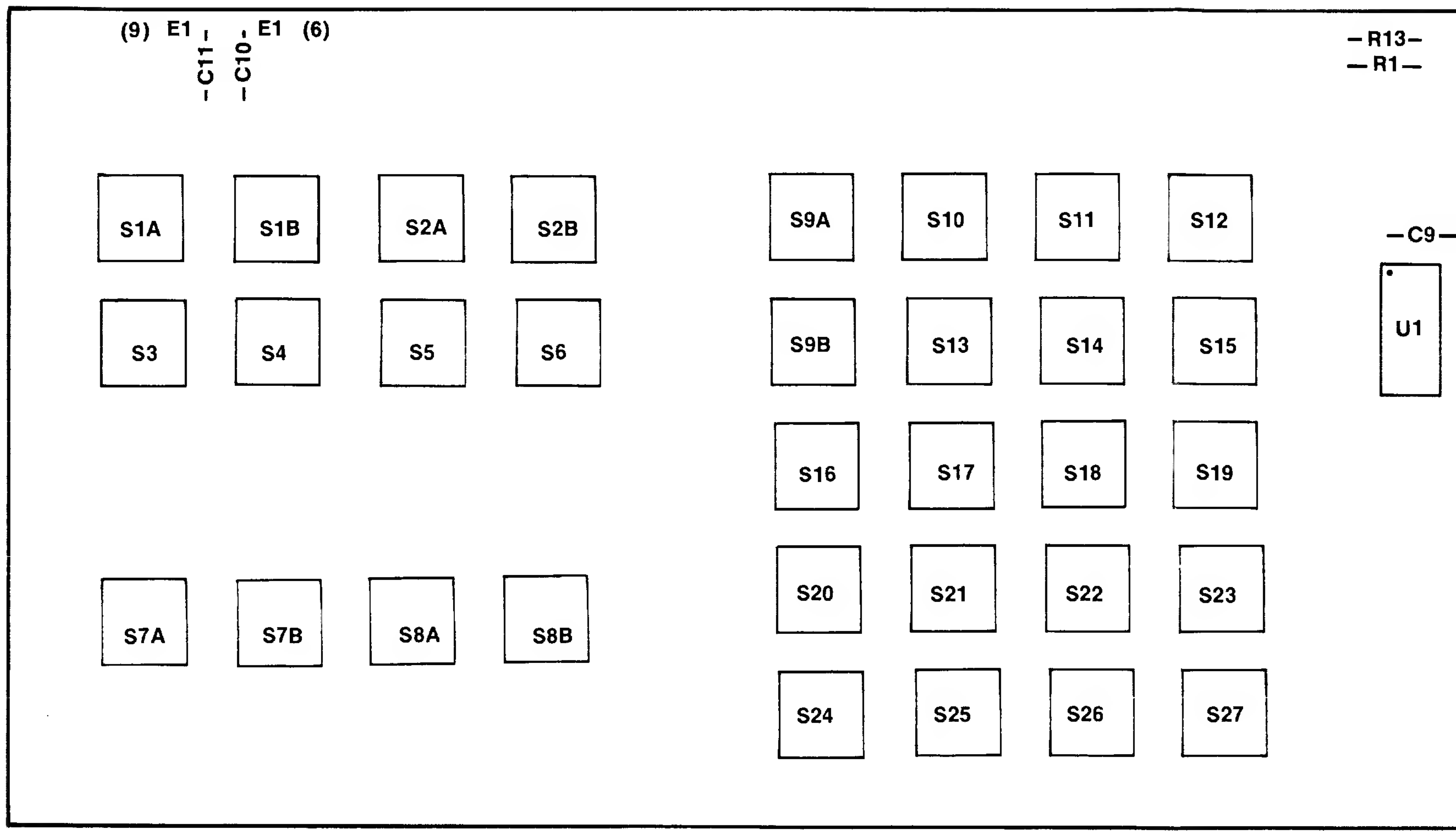


Figure 8-53. Block Diagram, Control Section for Schematic 9



U1, flux is
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Reset) is a
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grator out-
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one scan,

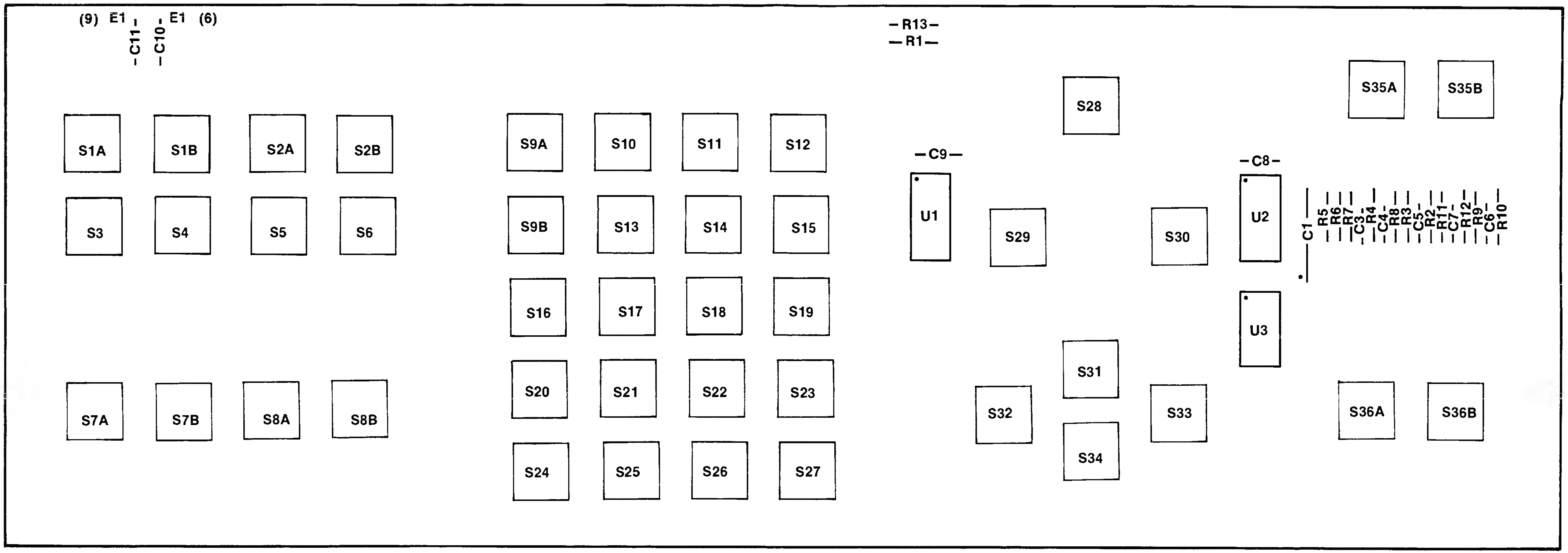
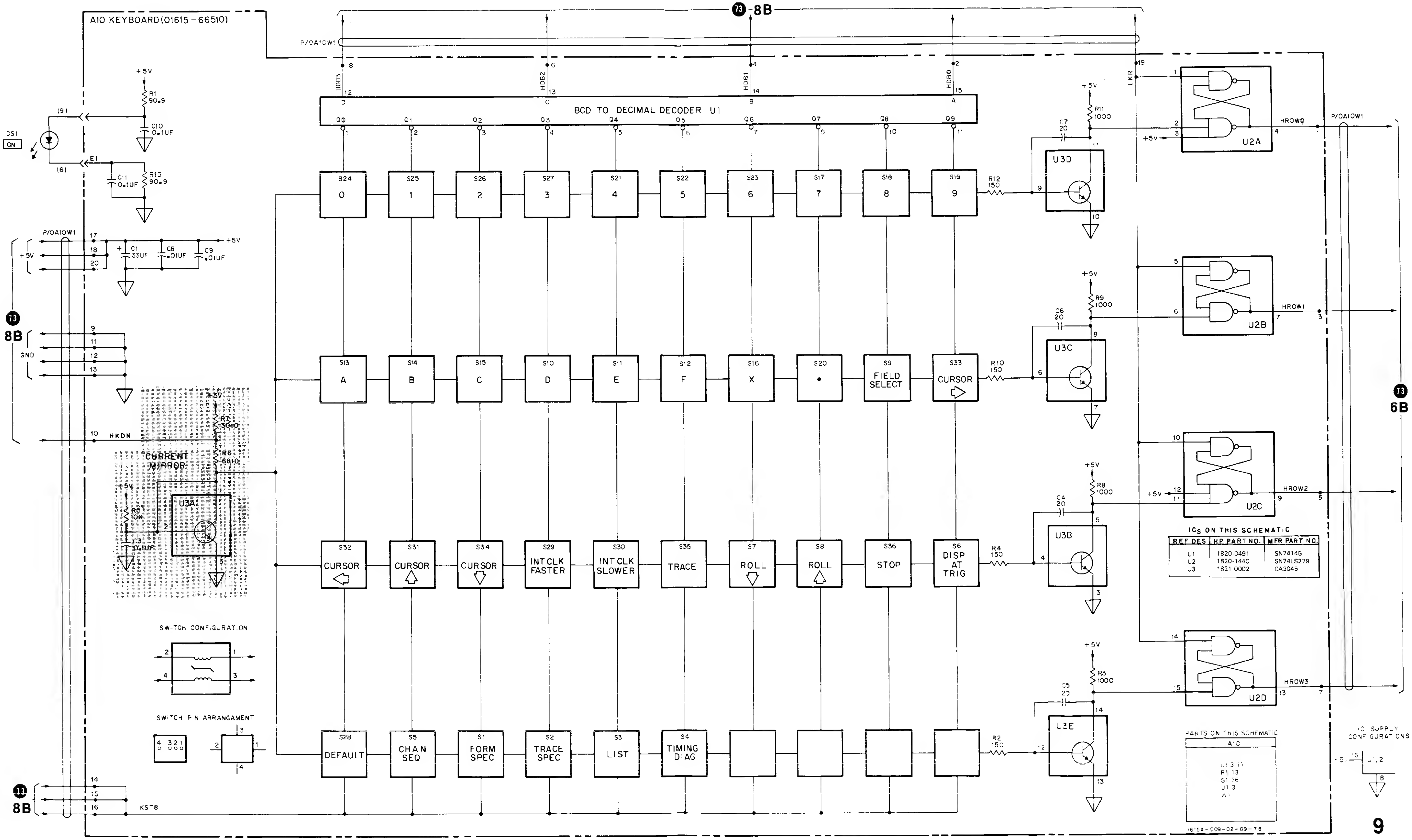


Figure 8-54. Keyboard Assembly A10. Parts Identification



REF DES	HP PART NO.	MFR PART NO.
U1	1820-0491	SN74145
U2	1820-1440	SN74LS279
U3	1821-0002	CA3045

Figure 8-55.
Keyboard A10 Schematic

SERVICE SHEET 10A

PRINCIPLES OF OPERATION

Dot and Retrace Counters. The 8-bit dot counters (U9 and U23) generate all of the horizontal dot locations across the face of the CRT (dot 0 on the left and dot 255 on the right). At the end of a line (dot 255), the terminal count from U23 increments the line counter (U37 and U51) and parallel enables the retrace counter (U11 and U10).

The retrace counter leaves its normal terminal-count state, assumes count 1100 0000, and starts counting PDCLK (Positive D Clock) clocks. This is the CRT retrace period. During the retrace period, the dot counter is disabled by a low from the retrace counter, and parallel loaded to 0000 0000. At the end of the retrace period, the retrace counter latches at terminal count, the dot counter begins counting out the next line, and the cycle repeats.

Vertical Presentation Control. The vertical area of the screen is divided into 255 horizontal raster lines. The line counter (U37 and U51), in conjunction with the vertical format ROM's (U50, U36, and U22), format the entire display. The 8-bit output from the line counters is decoded for each horizontal raster line in the vertical format ROMs. Each line must be treated as a special case: some lines are used for blanking, some for alphanumerics, some for either alphanumerics or timing diagrams, etc. The ROM stores the format for each line and configures this information into twelve lines of binary data for the raster line being presented.

Alphanumeric Displays. In alphanumeric presentations, each character is six dots wide by nine raster lines high. The sixth dot and the last two raster lines in each character are blanked to provide spacing between characters and lines.

The CRT face is divided into 800 character spaces, 40 character spaces along each line by 20 character lines. The first line at the top of the CRT contains characters 0 through 39, the next line contains characters 40 through 79, etc.

The character counters consist of U4 through U6. These count the 800 alphanumeric character spaces on the CRT face. During each horizontal sweep, they count up 40 characters. During eight out of every nine retrace periods, they count back down 40 characters. During every ninth retrace period, the count-down input is disabled so that the following character count will begin on the next line of 40 character spaces.

The character counters generate a 10-bit byte that addresses the display RAM. The same line of memory is addressed for each of the nine raster sweeps. Then the next line of memory is addressed for nine sweeps, etc. The vertical format ROMs select which raster line of the character will be represented during each of the nine sweeps.

NAND gate U25B supplies the count-up clock to the character counters. When LHB1 and LHB2 (Low Horizontal Blanking 1 and 2) are high, U25B connects NCHCLK (Negative-edge Character Clock) to the count-up inputs. During retrace, gates U12A and U12B supply the clocks for the count-down inputs.

Three binary outputs from the retrace counters are supplied to U12A. They are decoded to obtain exactly 39 clocks from U12A during retrace. These 39 clocks, plus the terminal count pulse from the dot counters, are supplied through U12B to drive the count-down input of the character counters. These 40 pulses return the character counters to the beginning of the line.

A high from VF2 (pin 10 of U50) is clocked through U38A to enable U12B during raster lines one through eight of each character. On the ninth raster line of each character, VF2 switches low and prevents transfer of the down-count clocks from U12A through U12B.

Alphanumeric Display/Timing Diagram Selector. The alphanumeric/time switch consists of U39C, U52A, and U46A. These switch logic levels which enable the alphanumeric circuitry and the timing diagram circuitry. The alphanumeric circuitry generates the heading, channel numbers, and data lists. The timing diagram circuitry generates the traces used during timing diagram presentations.

The HALPH, LALPH, and LALPH2, (High and Low Alphanumeric) signals will always be true, except in the CRT spaces where timing diagrams are permitted. In these spaces, VF0 (pin 12 of U50) is high. When timing diagrams have been selected, HTIME (High Timing Diagram) is high. When both of these signals are high, U39C provides a low state to the D input of U52A. This low switches the outputs of U52A and U46A to enable the timing diagram circuitry and disable the alphanumeric circuitry. When alphanumeric presentations are selected, HTIME is low. When in areas of the CRT display reserved for alphanumeric presentations (such as the heading), VF0 is low. Either low will force the alphanumeric/time switch to enable the alphanumeric circuitry and disable the timing-diagram circuitry.

Horizontal Blanking. The horizontal blanking logic consists of U24 and U25. At the beginning of a trace, the terminal count of the retrace counters is high, and LHB1, LHB2, and LHB3 (Low Horizontal Blanking 1, 2, and 3) are all high. These three blanking signals are combined on U24 to generate a signal called HHB (High Horizontal Blanking) which is low. Any one of the LHB1, 2, or 3 inputs can go low to generate HHB which blanks the CRT.

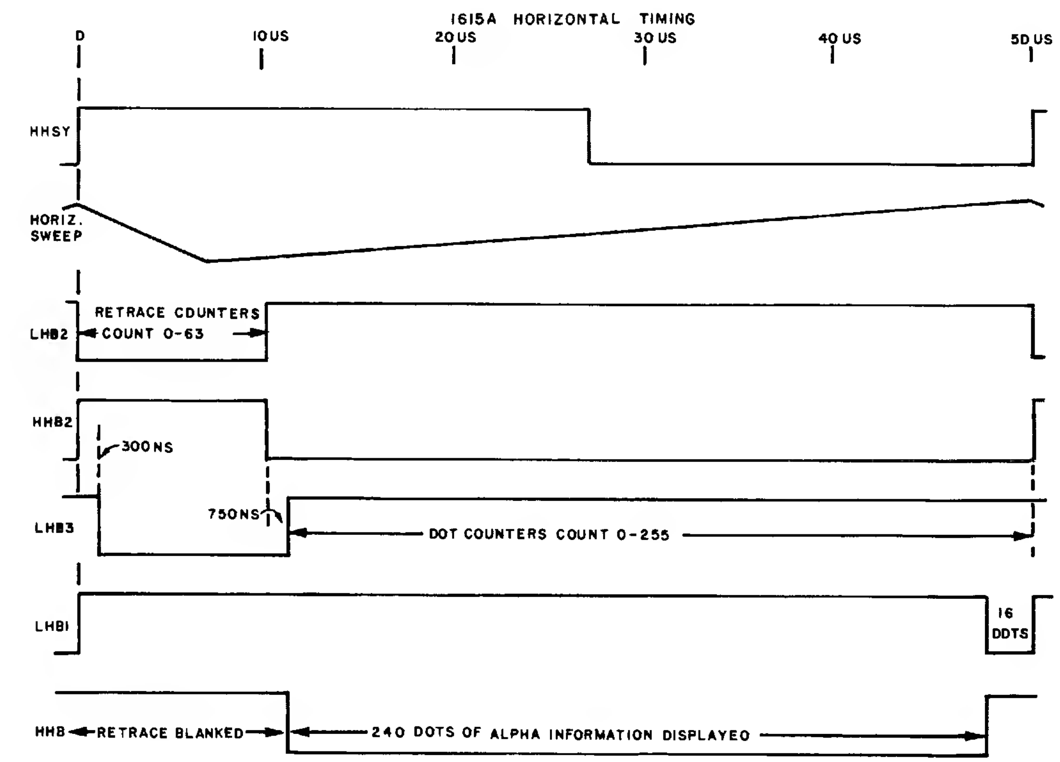
The blanking for the alphanumeric part of the diagram occurs after dot 240. This point is detected by U24A which sets LHB1 low. At count 255, the dot counters parallel enable the retrace counters and the terminal count of U10 is low, generating LHB2. LHB2 remains low for the horizontal retrace period. LHB2 maintains the HHB high to continue blanking, stops HHSY (High Horizontal Sync), and disables U25B to prevent NCHCLK (Negative Character Clock) from clocking the count-up input of the character counters.

One PCLK6 clock later, LHB3 goes low. This sets the alphanumeric/time switch to alphanumeric and continues the blanking of HHB from U24B.

When the retrace counters reach terminal count, even though the dot counters are no longer parallel enabled, they can not function due to LHB3 which remains low until the next PCLK6 clock is received from the microprocessor. This additional clock period after retrace permits all functions to be synchronized with the microprocessor clock. When PCLK6 arrives, LHB3 goes low, HHB goes low, and the dot counters begin a new cycle.

Horizontal Sync/Power Supply Sync. U25C, along with U39B and U39D, generate HHSY (High Horizontal Sync) which is used on assembly A13 to control the horizontal deflection circuit, and as a 20-kHz sync signal in the power supply.

Graticule Generator. The graticule generator consists of U52B and U53. It is a divide-by-20 counter that operates only during timing diagram generation. During alphanumeric presentations, U52B is cleared by a low LALPH which prevents operation. The graticule generator HGRAT (High Graticule) pulse occurs once every 20 dots during a timing diagram. U58B divides the NDCLK by 2 and decade counter U53 makes ten counts to terminal count. At the beginning of each line, U53 is parallel enabled and loaded with a binary 9. On the first clock after enable (High or LALPH), it generates the first HGRAT pulse. Then it generates a new HGRAT pulse every 20 clocks thereafter.



LHB1 - blanks after dot 240 to eliminate alphanumerics.

LHB2 - blanks during horizontal retrace. Stops HHSY. Prevents count-up in character counters.

LHB3 - sets alphanumeric/time switch to alphanumeric, and extends blanking period.

HHB - Composite of LHB1, LHB2, and LHB3.

HHSY - switches every half-sweep-cycle to control horizontal deflection in A13.

HHB2 - activates a gate on the microprocessor board that is used only during retrace in X10 magnification modes.

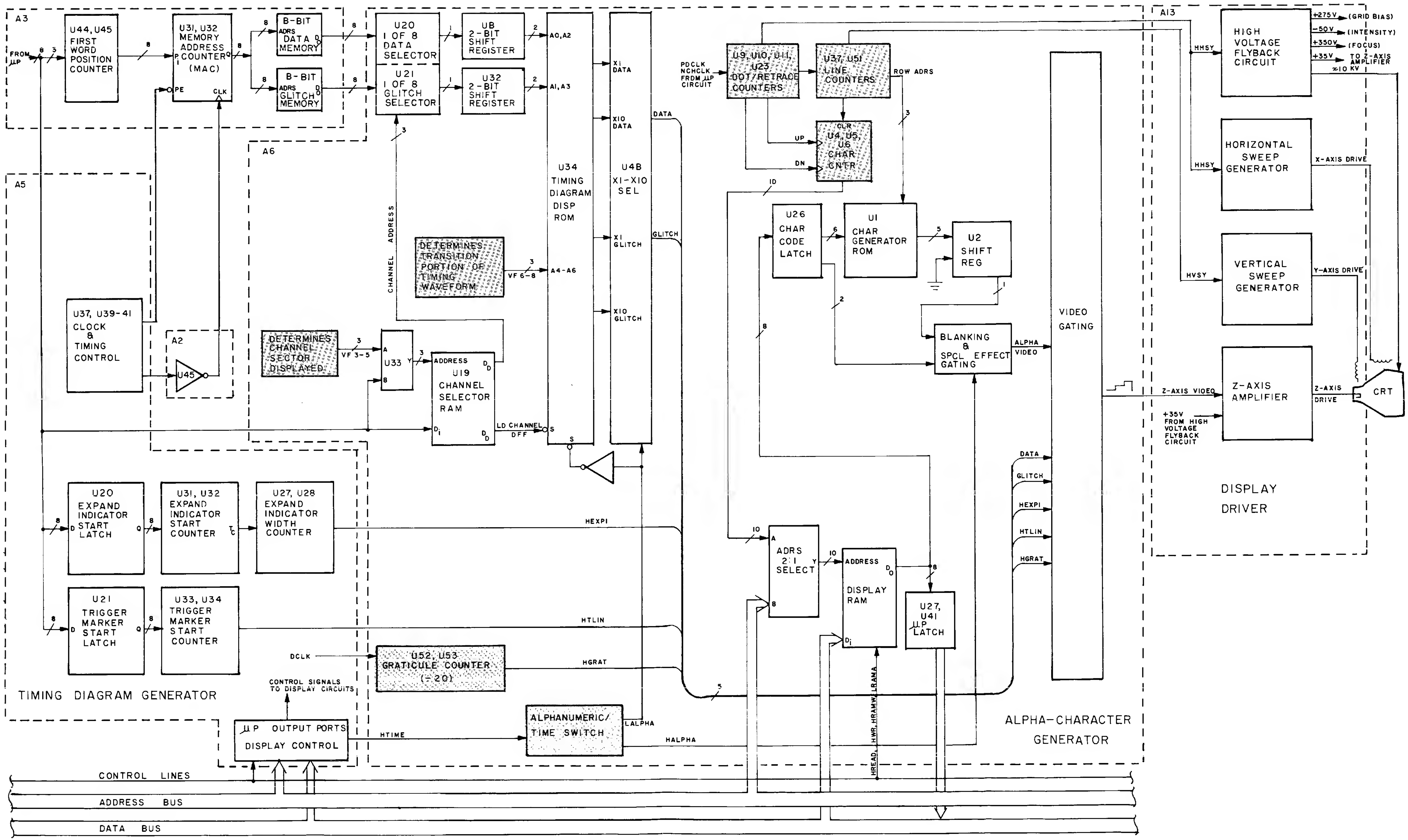
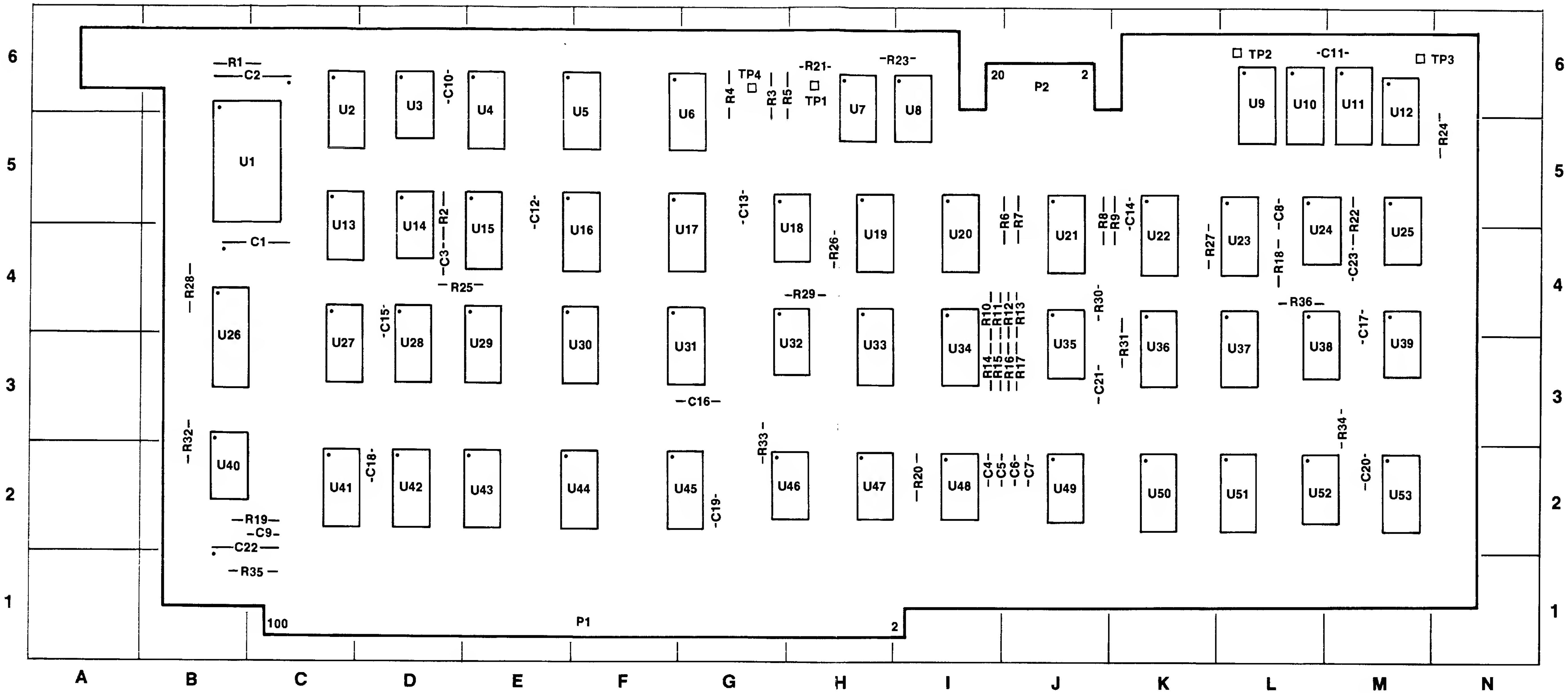
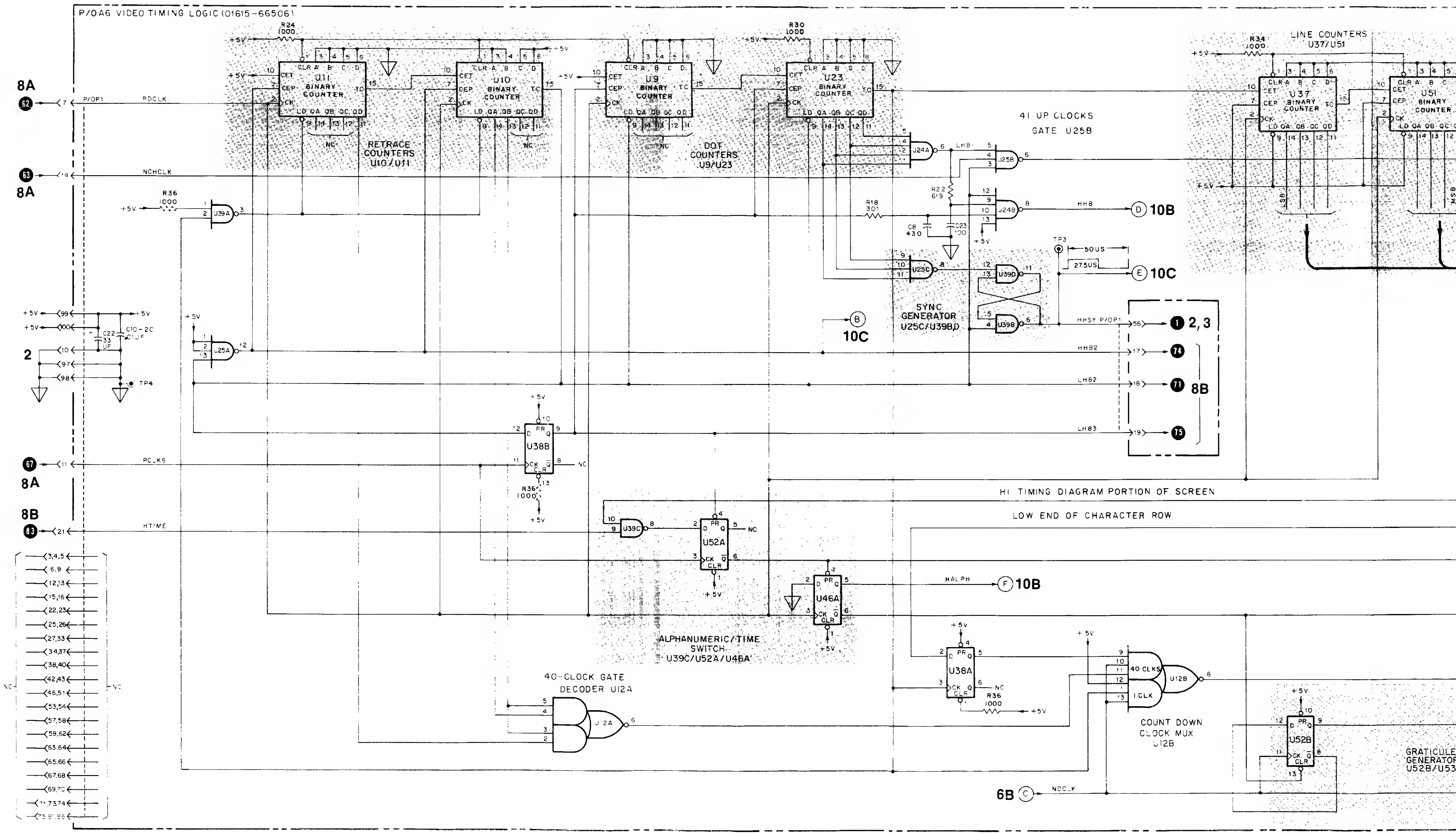


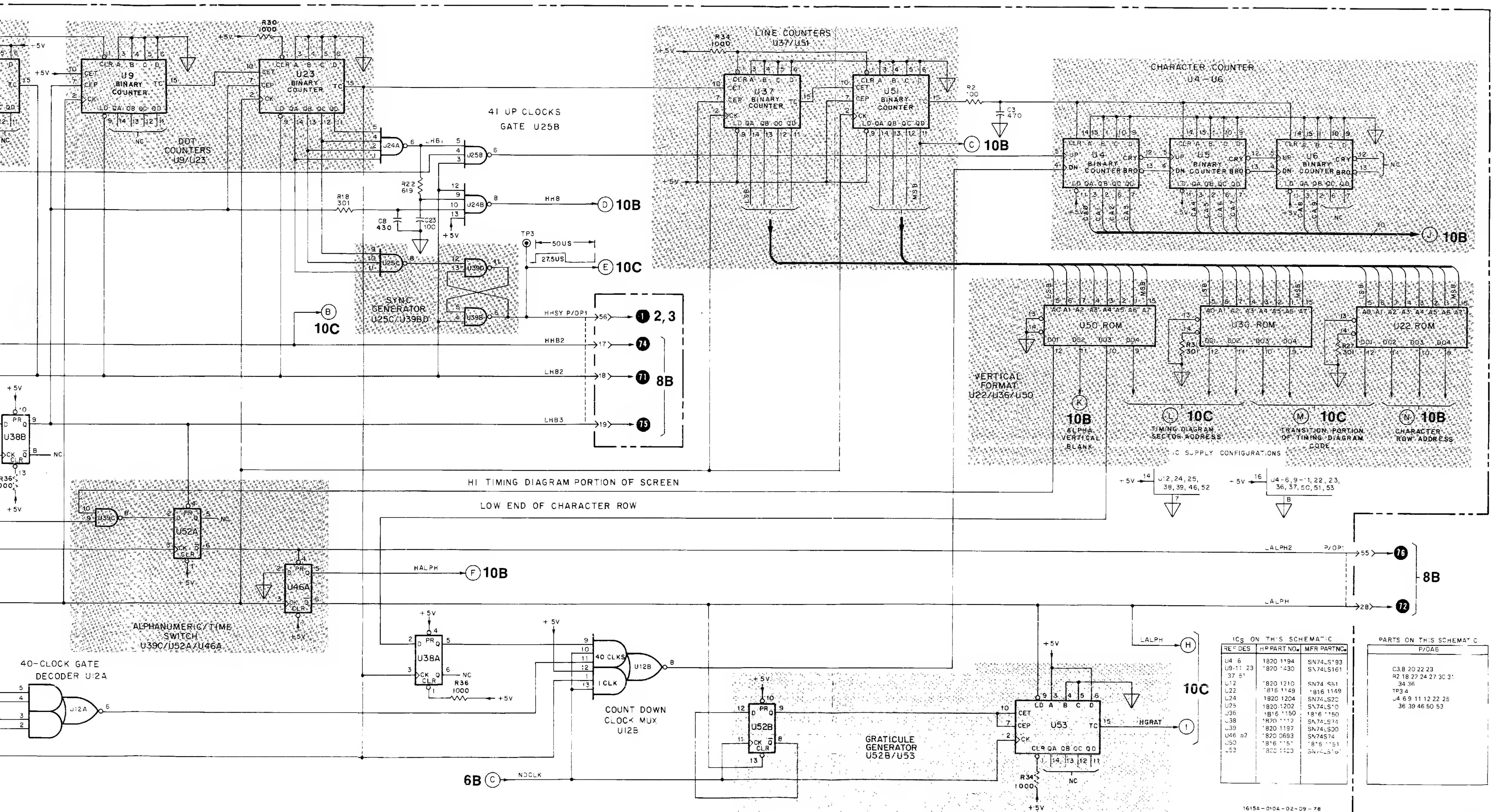
Figure 8-56.
Block Diagram, Display Section for Schematic 10A



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C-4	C16	G-3	R6	J-5	R21	H-6	R36	L-4	U11	M-6	U26	B-3	U40	8-2
C2	C-6	C17	M-4	R7	J-5	R22	M-5	TP1	G-6	U12	M-6	U27	C-3	U41	C-2
C3	D-4	C18	D-2	R8	J-5	R23	I-6	TP2	L-6	U13	C-4	U28	D-3	U42	D-2
C4	I-2	C19	G-2	R9	K-5	R24	N-5	TP3	M-6	U14	D-4	U29	E-3	U43	E-2
C5	I-2	C20	M-2	R10	I-4	R25	D-4	TP4	G-6	U15	E-4	U30	F-3	U44	F-2
C6	J-2	C21	J-3	R11	I-4	R26	H-4	U1	8-5	U16	F-4	U31	G-3	U45	G-2
C7	J-2	C22	8-2	R12	J-4	R27	K-4	U2	C-6	U17	G-4	U32	H-3	U46	H-2
C8	L-5	C23	M-4	R13	J-4	R28	B-4	U3	D-6	U18	H-4	U33	H-3	U47	H-2
C9	C-2	P1	F-1	R14	I-3	R29	H-4	U4	E-6	U19	H-4	U34	I-3	U48	I-2
C10	D-6	P2	J-6	R15	I-3	R30	J-4	U5	F-6	U20	I-4	U35	J-3	U49	J-2
C11	M-6	R1	8-6	R16	J-3	R31	K-3	U6	G-6	U21	J-4	U36	K-3	U50	K-2
C12	E-5	R2	D-5	R17	J-3	R32	B-2	U7	H-6	U22	K-4	U37	L-3	U51	L-2
C13	G-5	R3	G-6	R18	L-4	R33	G-2	U8	I-6	U23	L-4	U38	L-3	U52	L-2
C14	K-5	R4	G-6	R19	C-2	R34	M-3	U9	L-6	U24	L-4	U39	M-3	U53	M-2
C15	D-4	R5	G-6	R20	I-2	R35	C-1	U10	L-6	U25	M-4				

Figure 8-57. Display Programmer Assembly A6, Parts Identification


P/OA6 VIDEO TIMING LOGIC (01615-66506)
RETRACE COUNTERS U10/U11
DOT COUNTERS U9/U23
41 UP CLOCKS GATE U25B
LINE COUNTERS U37/U51
SYNC GENERATOR U25C/U39B,D
HI TIMING DIAGRAM PORTION OF SCREEN
LOW END OF CHARACTER ROW
ALPHANUMERIC/TIME SWITCH U39C/U52A/U46A
40-CLOCK GATE DECODER U12A
COUNT DOWN CLOCK MUX U12B
GRATICULE GENERATOR U52B/U53
PDCLK
NCHCLK
PCLK5
HTIME
HHB
HHSY P/OP1
HHB2
LHB2
LHB3
HALPH
NDCLK
8A
8B
10B
10C
6B
2, 3



10A

Figure 8-58.
Video Timing Logic (P/O A6) Schematic

SERVICE SHEET 10B

PRINCIPLES OF OPERATION.

Data Selectors and RAM. Data selectors U15 through U17 connect ten lines of address from either the microprocessor or character counters to the RAM (U28 through U31 and U42 through U45). When HUPC (High Microprocessor Control) is high, the microprocessor addresses the RAM; when low, the character counters address the RAM.

Alphanumeric Latch. Alphanumeric latch U26 receives the RAM outputs. The first six bits are the ASCII code for the alphanumeric character to be presented. The last two bits control the display format, selecting normal video, inverse video, and blinking video.

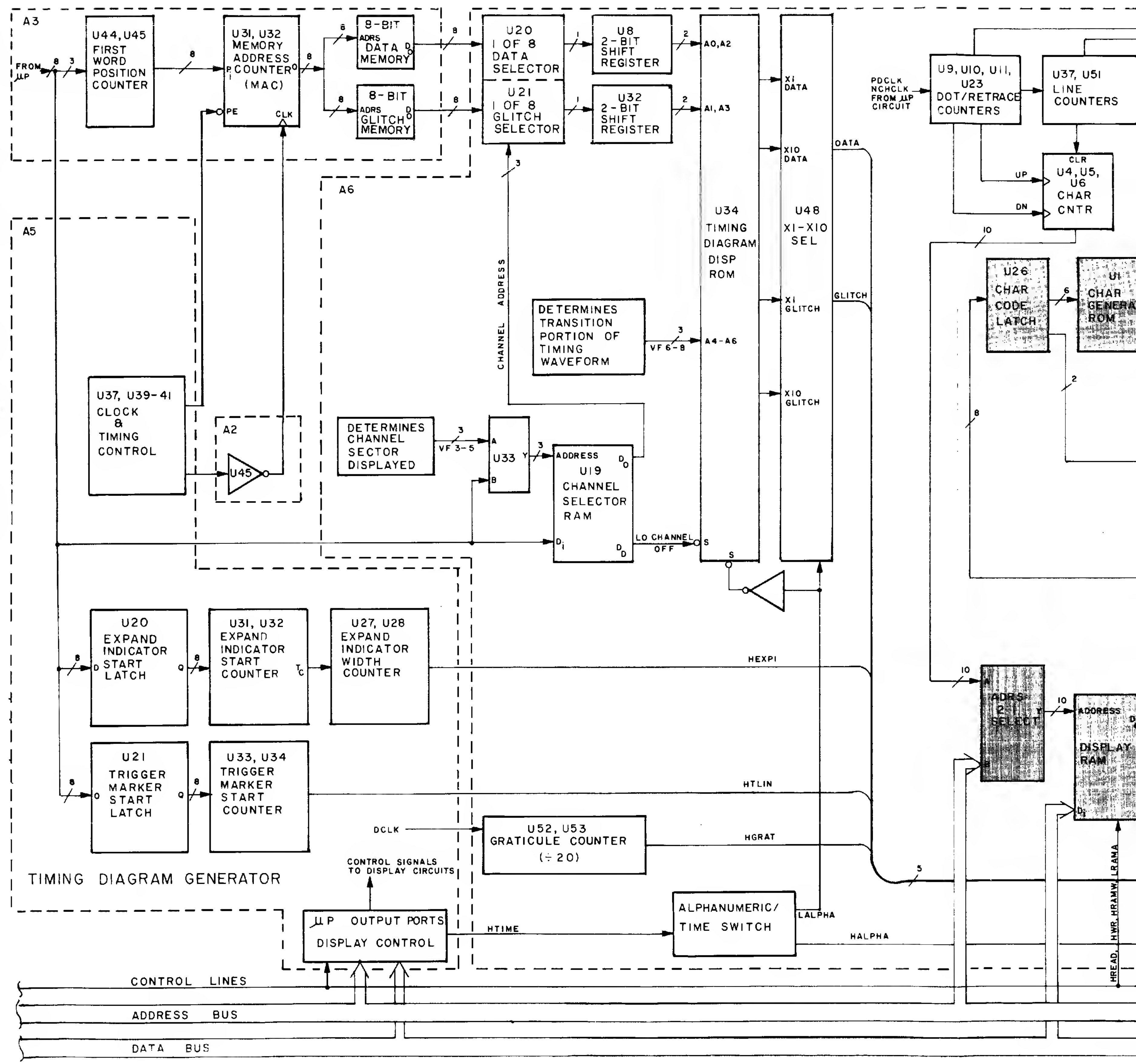
Character ROM/Shift Register. The ASCII character code in U26 is supplied to U1. Vertical format bits VF9 through VF11 are decoded to select the particular raster line (0 through 6) of the character to be displayed. U1 parallel loads the proper binary information into U2 for the raster line to be presented. The U2 inputs that are tied low are used for blanking between characters. The raster-line data from U1 is parallel loaded into U2 when the shift/load input of U2 is low. This occurs when NDCLK is high and PDCLK1 is low (time between characters).

Alphanumeric Output Multiplexer. U3 consists of four AND gates NORed together. With all AND outputs low, the NOR output is high. This brightens the CRT at the corresponding point. When any AND gate in U3 is high, pin 8 of U3 is low, blanking the corresponding point on the CRT.

The top AND gate of U3 accepts the inputs for normal video. The next AND gate provides blanking when required by HHB (High Horizontal Blanking). The third AND gate accepts the inputs for inverse video. The bottom AND gate receives VF1 from the vertical format ROM. This gate controls raster line blanking. HALPH (High Alphanumeric) enables U3 during alphanumeric displays and forces the output of U3 high during timing diagram displays.

RAM Output Latches. Latches U27 and U41 are D latches with three-state outputs. Since G1 and G2 are low, the latches are always enabled. The 8-bit data from RAM are latched on every positive clock. Normally the latch outputs are in the high-impedance state. To place the latched information on the data bus, the microprocessor sets HREAD (High Read) high and LRAMA (Low RAM Address) low. This forces output control pins 1 and 2 both low on U27 and U41.

RAM Write Logic. When LRAMA is low, HWR (High Write) is high, and HRAMW (High RAM Write) is high, U47C enables the RAM WRITE terminals. This enters the data from the data bus into the RAM at the locations addressed by U15 through U17.



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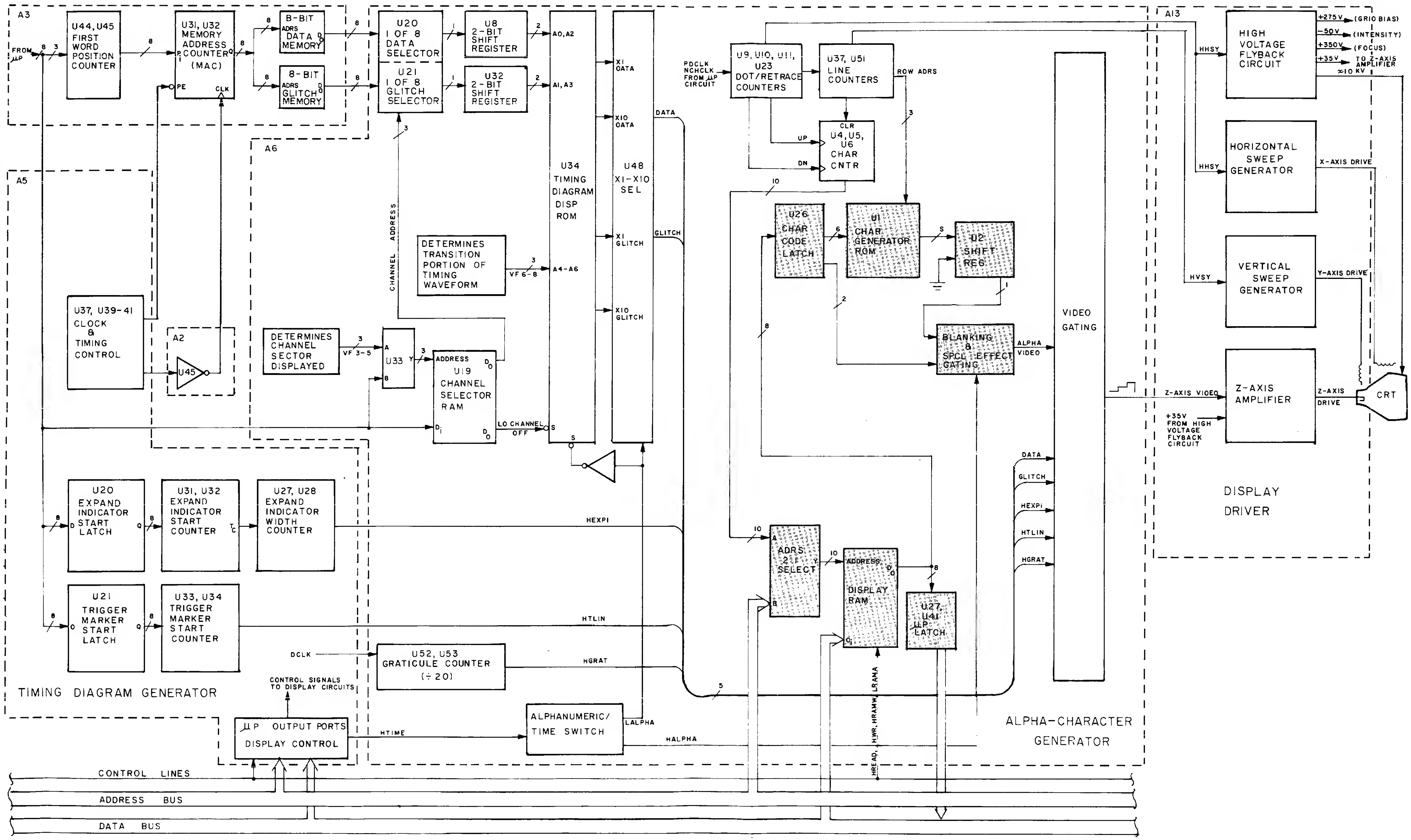


Figure 8-59. Block Diagram, Display Section for Schematic 10B

SIGNATURE ANALYSIS FOR SCHEMATIC 10B.

The signatures on this schematic are obtained by using DSA Setups A, C, and D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A6 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A6, and install A6 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ↓
STOP.................................... ↑
CLOCK .... ↓

Signatures for DSA Setup A (Schematic 10B)

Pin	Signature	Pin	Signature
VH A6U1-24	C690	A6U41-3	FHPA
A6U27-3	C43H	A6U41-4	57CA
A6U27-4	C6P3	A6U41-5	08F5
A6U27-5	FA2P	A6U41-6	AHA3
A6U27-6	427H	A6U42-11	AHA3
A6U28-11	427H	A6U43-11	08F5
A6U29-11	FA2P	A6U44-11	57CA
A6U30-11	C6P3	A6U45-11	FHPA
A6U31-11	C43H		

DSA SETUP C.

1. Remove assembly A6 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A6, and install A6 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   d. Connect signature analyzer stop line to same point as start line, step c above.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 part number is 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ↑
STOP.................................... ↑
CLOCK .... ↓

Signatures for DSA Setup C (Schematic 10B)

Pin	Signature
VH A6U1-24	0001
A6U15-10	UUUU
A6U15-13	5555
A6U16-3	CCCC
A6U16-6	7F7F
A6U16-10	5H21
A6U16-13	0AFA
A6U17-3	UPFH
A6U17-6	52F8
A6U17-10	HC89
A6U17-13	2H70
A6U27-1	2AU9
A6U27-1	1920*
A6U27-1	P43A**
A6U27-2	0000 (blinking)
A6U41-1	2AU9
A6U41-1	1920*
A6U41-1	P43A**
A6U41-2	0000 (blinking)
A6U47-11	2AU8
A6U47-11	1921*
A6U47-11	P43C*
A6U49-10	0000 (blinking)
A6U49-11	0001 (blinking)

*When A5 is 01615-66505 and HP-IB option not installed.
**When A5 is 01615-66505 and HP-IB option is installed.

DSA SETUP D.

1. Remove assembly A6 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A6, and install A6 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   c. Connect signature analyzer stop line to same point as start line, step b above.

   d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{WR}$ line.

4. Reinstall A5 in 1615A mainframe.

NOTE

DSA jumper on A5 remains in NM (normal) position in this test setup.

5. Set up signature analyzer as follows:

START .... ∫
STOP...................................... ∫
CLOCK.................................... ∫

Signatures for DSA Setup D (Schematic 10B)

Pin	Signature
VH A6U1-24 A6U47-10	0001 0001 (blinking)

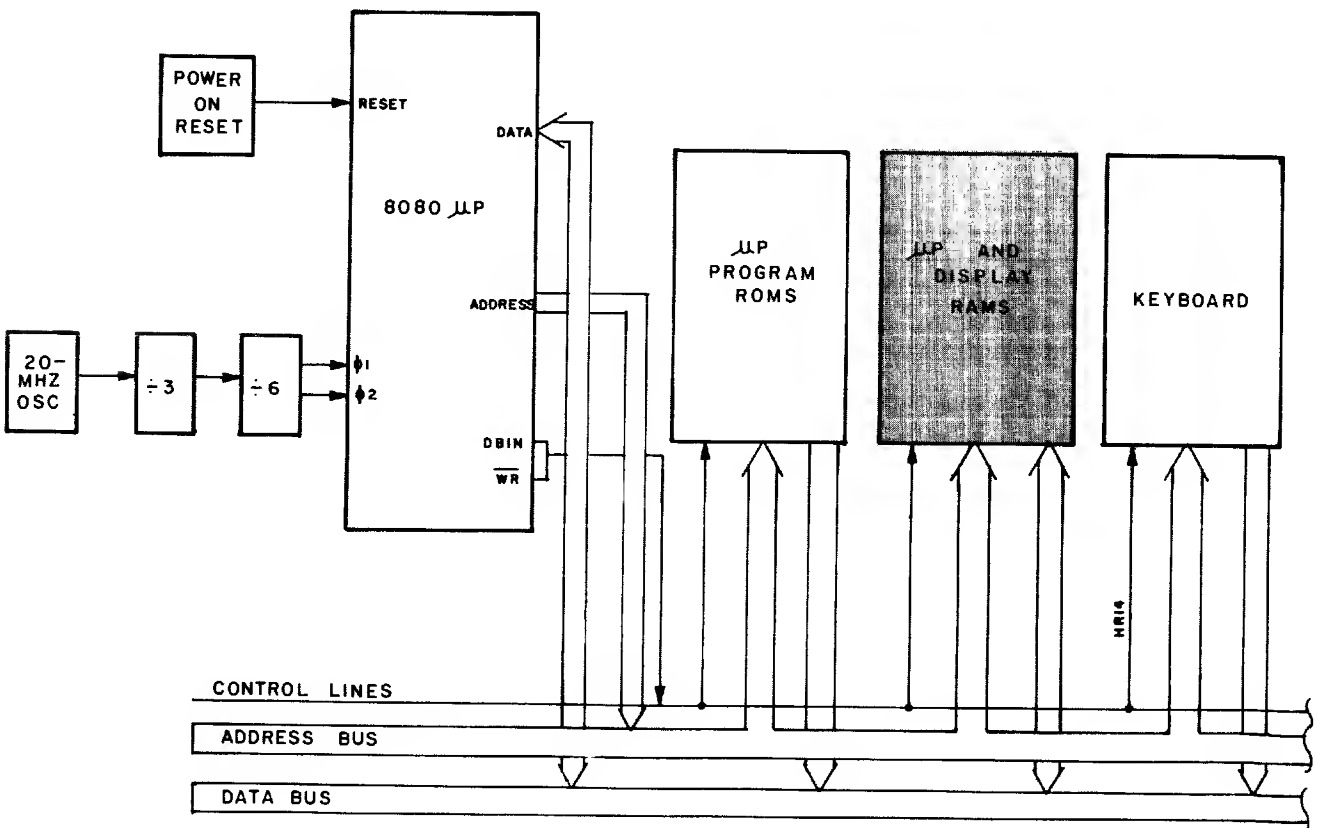
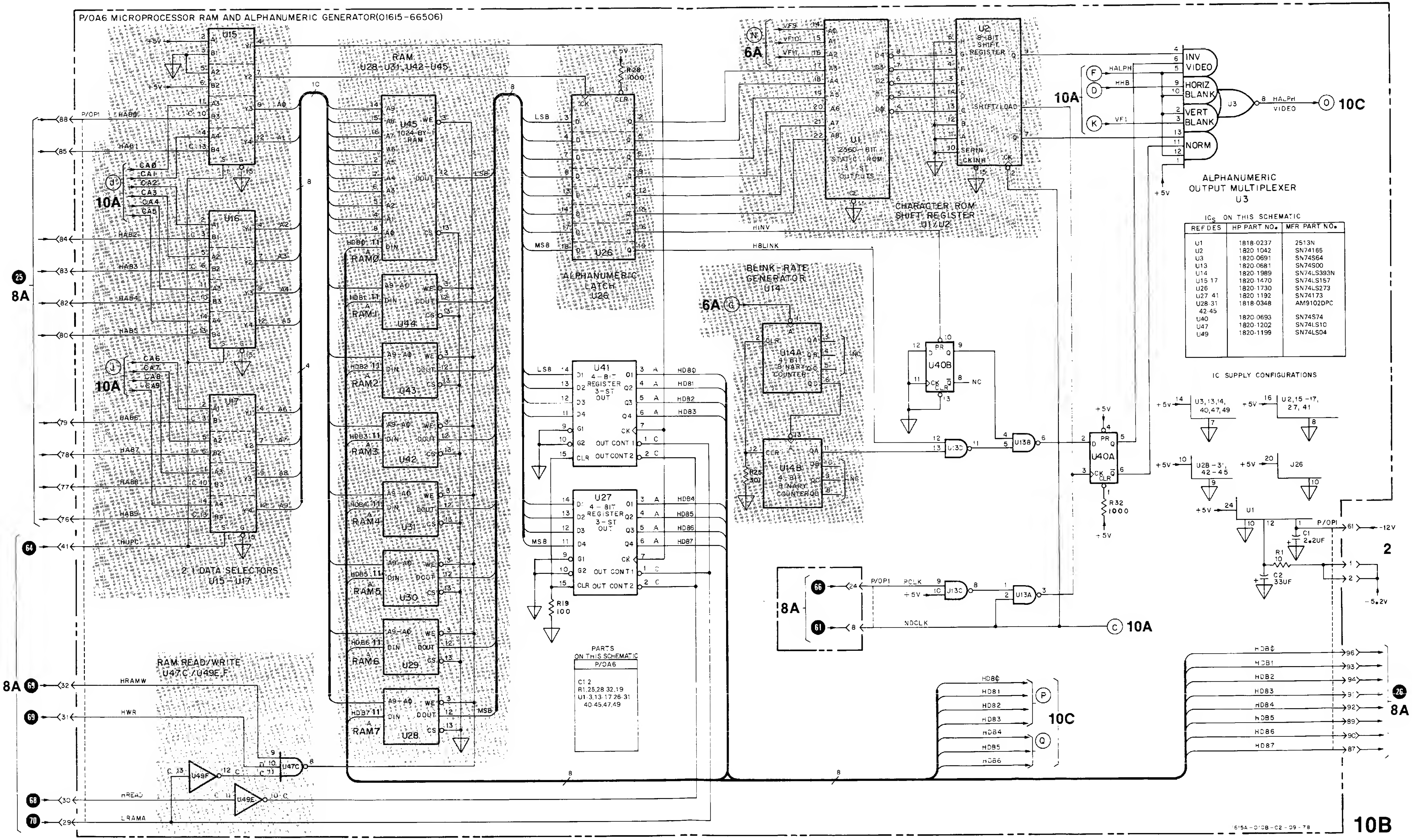


Figure 8-60. Block Diagram, Control Section for Schematic 10B



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1	1818-0237	2513N
U2	1820 1042	SN74165
U3	1820-0691	SN74S64
U13	1820-0681	SN74S00
U14	1820-1989	SN74LS393N
U15 17	1820-1470	SN74LS157
U26	1820-1730	SN74LS273
U27 41	1820 1192	SN74173
U28-31 42-45	1818-0348	AM9102DPC
U40	1820-0693	SN74S74
U47	1820-1202	SN74LS10
U49	1820-1199	SN74LS04

Figure 8-61.
Microprocessor RAM and Alphanumeric Generator (P/O A6) Schematic

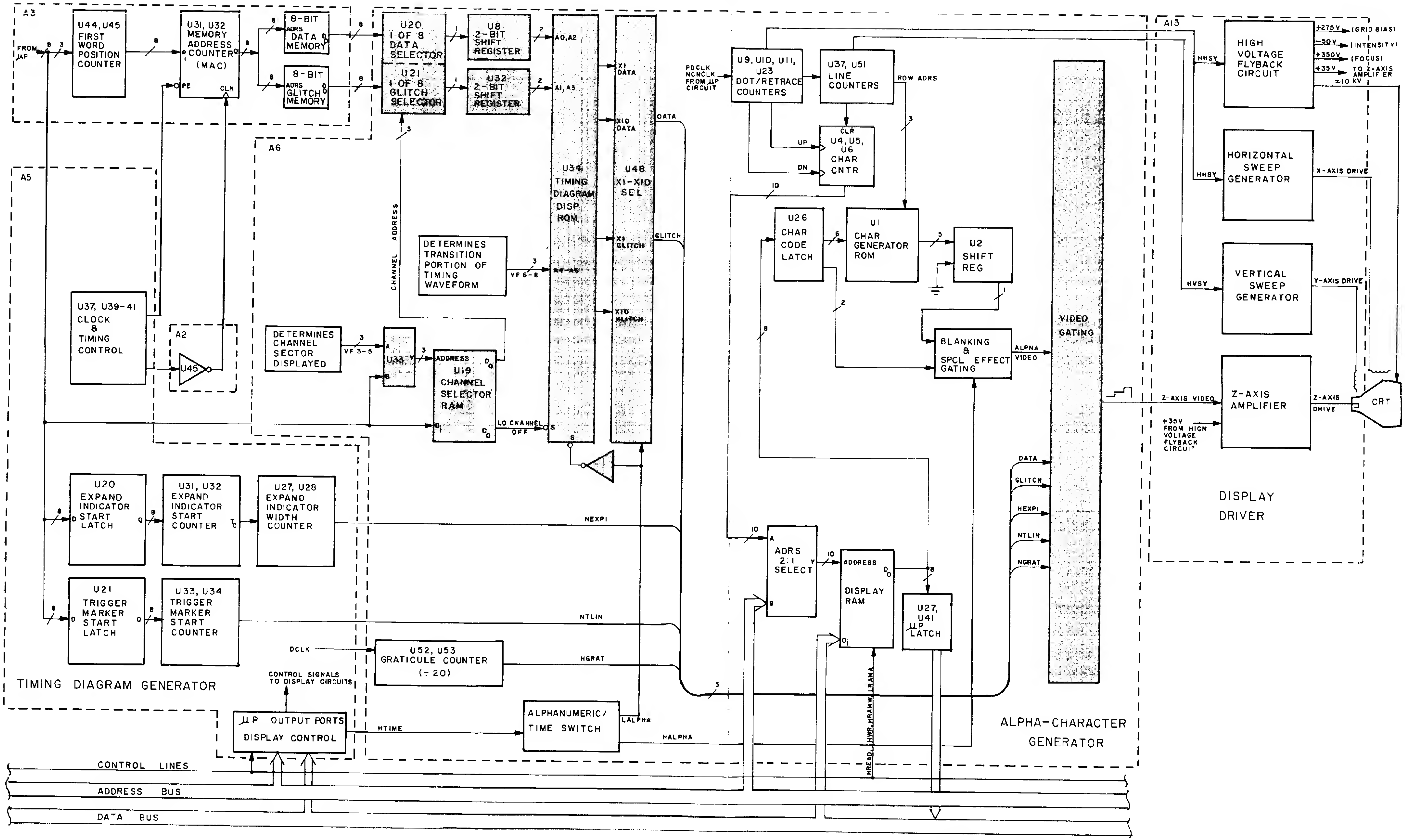


Figure 8-62. Block Diagram, Display Section for Schematic 10C

SERVICE SHEET 10C

PRINCIPLES OF OPERATION

Data Multiplexer. Multiplexer U20 receives the data from the 8-bit data memory on A3. U21 receives the eight lines of glitch information from the glitch memory. U20 is always active because its strobe (pin 7) is low. U21 is active only when LGL (Low Glitch) is low, glitch presentations are selected for the timing diagram.

The timing diagram is normally presented with channel 0 in the first CRT location. The other channels are presented in sequence, with channel 7 in the last CRT location. The sequence of presentation is controlled by U19 and U33. It can be rearranged by the 1615A operator through menu selection. For example, the operator may elect to display channel 4 in the first location, channel 6 in the second location, and blank the third location. These menu selections are entered into memory and loaded into U19 and U33 by the microprocessor.

Before each run, RAM U19 is loaded with the numbered channel to be presented at each of the eight timing diagram locations. VF3 through VF5 from the vertical format ROM indicate the timing diagram location being addressed on the CRT. RAM U19 obtains the present location from U33 and selects the channel number to be presented according to the program from the microprocessor. The first three bits from U19 select one of the eight data and glitch channels in U20 and U21. The fourth bit from U19 blanks the timing diagram in channels that were turned off. An X is displayed in the channel number column beside each blanked timing diagram location.

HSTD (High Start Timing Diagram) controls selection in U33. When HSTD is low, data bus inputs address locations in RAM U19 that contain the channel numbers. When HSTD is high, VF3 through VF5 select a data and glitch channel for the timing diagram.

Data and Glitch Latches. The information from the data and glitch channel selected in U20 and U21 is latched into U8B and U32A by the PDCLK (Positive D Clock). The outputs from U8B and U32A are applied to display ROM U34 where they are interpreted as instantaneous data and glitch. U8A and U32B latch this information on the next PDCLK. They supply their outputs to U34 where they are interpreted as the previous two bits.

Display ROM. The display ROM uses the present data and last data information to detect changes in levels (transitions). Vertical format bits VF6 through VF8 are decoded in U34 to identify each raster line in the timing diagram location being displayed. ROM U34 uses the above information to format the timing diagram. All points where the data are high have brightened dots on the top raster line. All points where the data are low have brightened dots on the bottom raster line. All points which include transitions (changes from low to high or high to low) have brightened dots on each raster line. The last two raster lines in each timing diagram location are reserved for blanking between channels.

Any time that U47B receives a low input, it deselects display ROM U34. The low input may come from several sources, depending upon the mode of operation. During alphanumeric displays, LALPH (Low Alphanumeric Display) is low. The fourth bit from U19 is supplied to U47B to blank particular timing diagram locations. HSTD is low when the channel number is being written. This clears U46B which places a low on U47B.

Outputs D1 (data) and D2 (glitch) from ROM U34 carry the information for the unexpanded (X1) display mode. D3 and D4 are the outputs for the expanded (X10) display mode. U48B gates the data information and U48A gates the glitch information from U34. Only one AND gate in U48A and U48B is enabled at one time. HX1 (High X1) and LX1 (Low X1) from the microprocessor make the selection according to display magnification selections made by the 1615A operator. When alphanumeric displays are being generated, U48B is disabled by a low LALPH. In this case, U48B provides a high output, enabling U7C to be controlled by HALPHVIDEO (High Alphanumeric Video) from the alphanumeric generator.

Output Gating. U18A, U18B, and U18C control display brightness for each data and glitch bit and graticule line presented on the CRT. The three U18 gates are open-collector AND gates. When any U18 gate receives a low input, it draws current across its associated resistor, lowering the voltage in the video output. This brightens the corresponding point on the CRT. The different resistor values in the gates of U18 are chosen to provide different levels of brightness for data bits, graticule line bits, and glitch bits.

U18B gates alphanumeric and timing-diagram data. It also gates the information for the trigger line tics when HTLIN (High Trigger Line) goes high during a timing diagram.

U18C gates the graticule lines on timing diagrams. U49C blanks graticule dots that occur within the time segment where a data dot is presented. This prevents excessive brightening of a single dot.

U18A gates glitch information and the expand indicator. It prevents double brightening when a glitch occurs within the brightened expand indicator. U47A NORs the expand indicator with the data line to restrict the expand indicator to that part of the trace which also includes data.

Contrast R21 is adjusted for the best contrast between data, graticule, and glitch information.

The HVSY (High Vertical Sync) pulse is generated on assembly A6. It is supplied to display driver A13 where it initiates vertical sweep.

SIGNATURE ANALYSIS FOR SCHEMATIC 10C.

The signatures on this schematic are obtained by using DSA Setups A and D. The red letters on the schematic signify the DSA setup to use when observing the signature on the adjacent IC pin. Setups and signatures are listed below. For further information, refer to TROUBLESHOOTING WITH SIGNATURE ANALYSIS at the beginning of this Section.

DSA SETUP A.

1. Remove assembly A6 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A6, and install A6 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Find DSA jumper beside microprocessor. Remove DSA jumper from NM (normal) terminals and reinstall it in the SA terminals.

   c. Connect signature analyzer start line to A5U1 pin 15.

   d. Connect signature analyzer stop line to A5U1 pin 10.

   e. Connect signature analyzer clock line to A5TP8 (use pin 17 of A5U11 if A5 is part number 01615-66505). This is the DBIN line from the microprocessor.

4. Reinstall A5 in 1615A mainframe.

5. Set up signature analyzer as follows:

START .... ˥
STOP .... ſ
CLOCK .... ˥

Signatures for DSA Setup A (Schematic 10C)

Pin	Signature	Pin	Signature
VH A6U1-24	C690	VH A6U19-12	AHA3
A6U19-4	FHPA	A6U33-2	C43H
A6U19-6	57CA	A6U33-5	C6P3
A6U19-10	08F5	A6U33-11	FA2P

DSA SETUP D.

1. Remove assembly A6 and the extender board from the 1615A mainframe.

2. Install the extender board in the connector for A6, and install A6 on the extender.

3. Remove microprocessor board A5 from the 1615A mainframe and proceed as follows:

   a. Remove A5U12 and A5U24.

   b. Connect signature analyzer start line to A5TP9 (use pin 36 of A5U11 if A5 part number is 01615-66505). This is address bit A15.

   c. Connect signature analyzer stop line to same point as start line, step b above.

   d. Connect signature analyzer clock line to pin 18 of A5U11. This is the microprocessor $\overline{WR}$ line.

4. Reinstall A5 in 1615A mainframe.

NOTE

DSA jumper on A5 remains in NM (normal) position in this test setup.

5. Set up signature analyzer as follows:

START .... ⌋
STOP .... ſ
CLOCK .... ſ

Signatures for DSA Setup D (Schematic 10C)

Pin	Signature
VH A6U1-24	0001
A6U7-1	755P

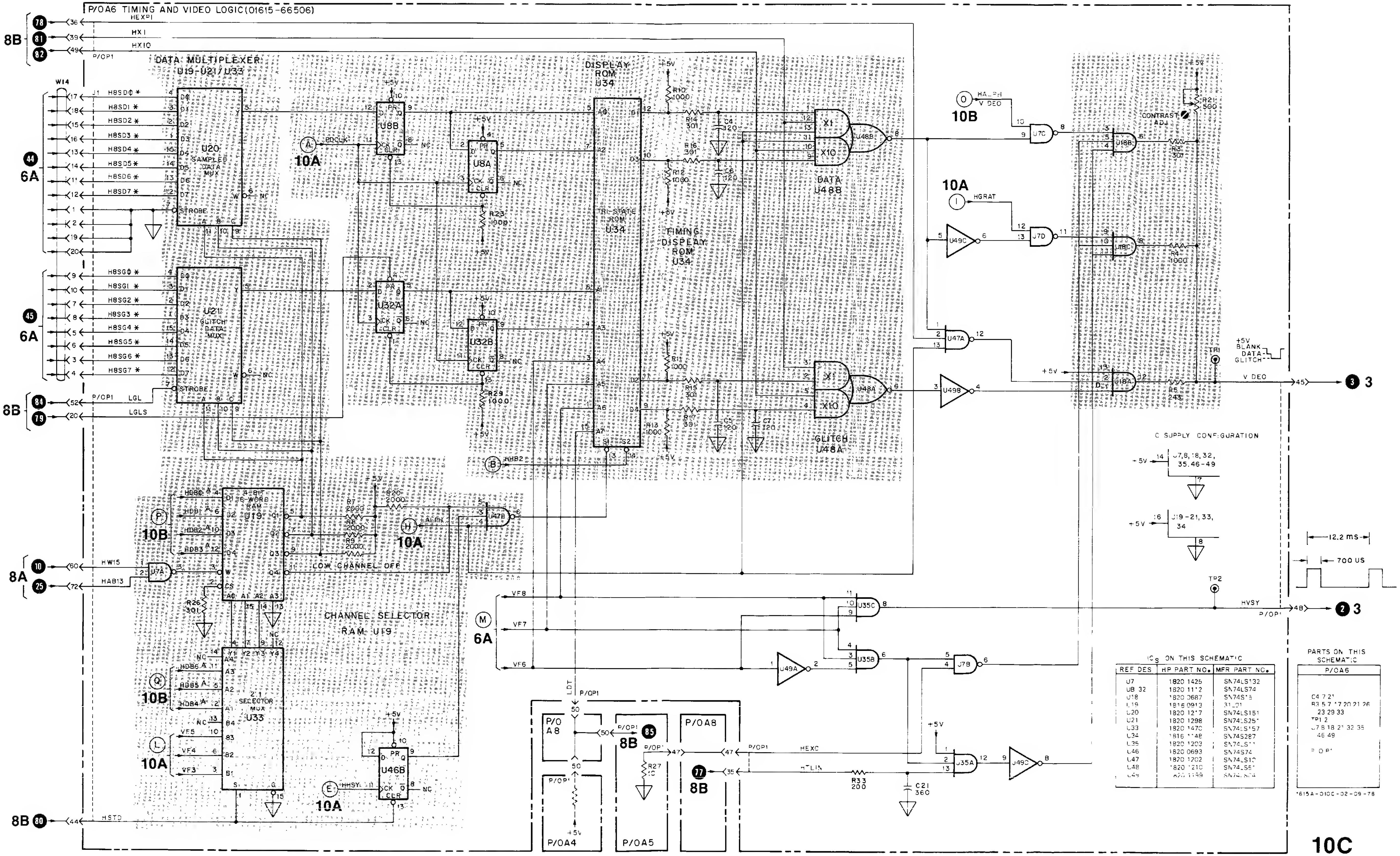


Figure 8-63.
Timing and Video Logic (P/O A6) Schematic

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